SA9312L USB Audio Streaming Controller

1. Features

- Supply Range of 1.8 V to 3.3 V
- Control and I/O
  - I2C bus
  - FWIOs
- Support iAP2 SA9312L
- USB 2.0 High-Speed Compliant
- USB Audio Class v1.0 and v2.0 supported
- Support Dynamic Consumption Adjustment
- One interrupt endpoint for HID
- Support DSD64 / DSD128 / DSD256 both of native and DoP in Async mode
- Support DSD L/R data line swap feature
- Support resolutions up to 32-bit and sampling rates up to 384KHz
- Support fixed DMCLK mode
  - 11.2896/ 12 / 12.288 / 22.5792/ 24.576MHz
- One I2S input and one I2S output pairs for PCM
  - Independent sample rates for each pair
  - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384 KHz sampling rates
  - 16/24/32-bit resolution
- 49-pin WLCSP package

2. Description

- Mobile Phone Audio Accessary
- Type-C Audio
- USB Audio

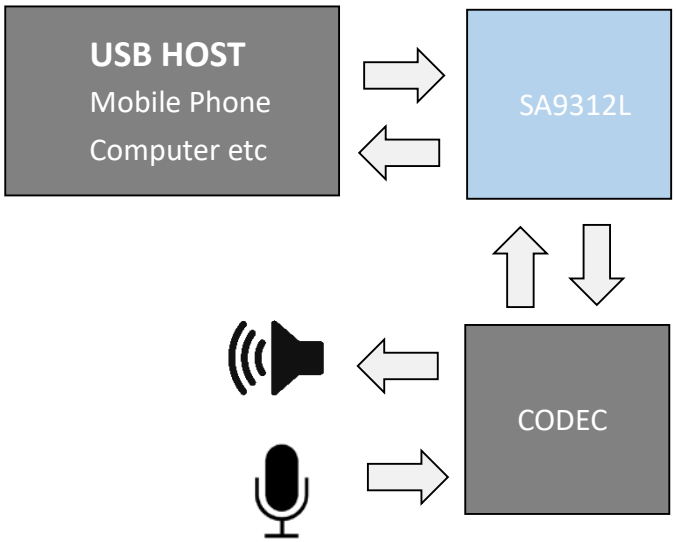
3. Applications

The SA9312L is a high-performance up to 32bit, 384KHz PCM and DSD64/128/256 streaming USB High-Speed compliant audio steaming controller. It features one IEC60958 S/PDIF transmit streaming output. The SA9312L is ideal for both one stereo-in and one stereo-out professional digital audio interface applications. Its PCM resolution and sampling rate can be configurable with 16/24/32

Device Information

PART NUMBER	PACKAGE	BODY SIZE
SA9312L	WLCSP	3.53mm x 3.53mm

4. Simplified Schematic



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5. Pin Configuration and Functions

5.1 Pin Configuration

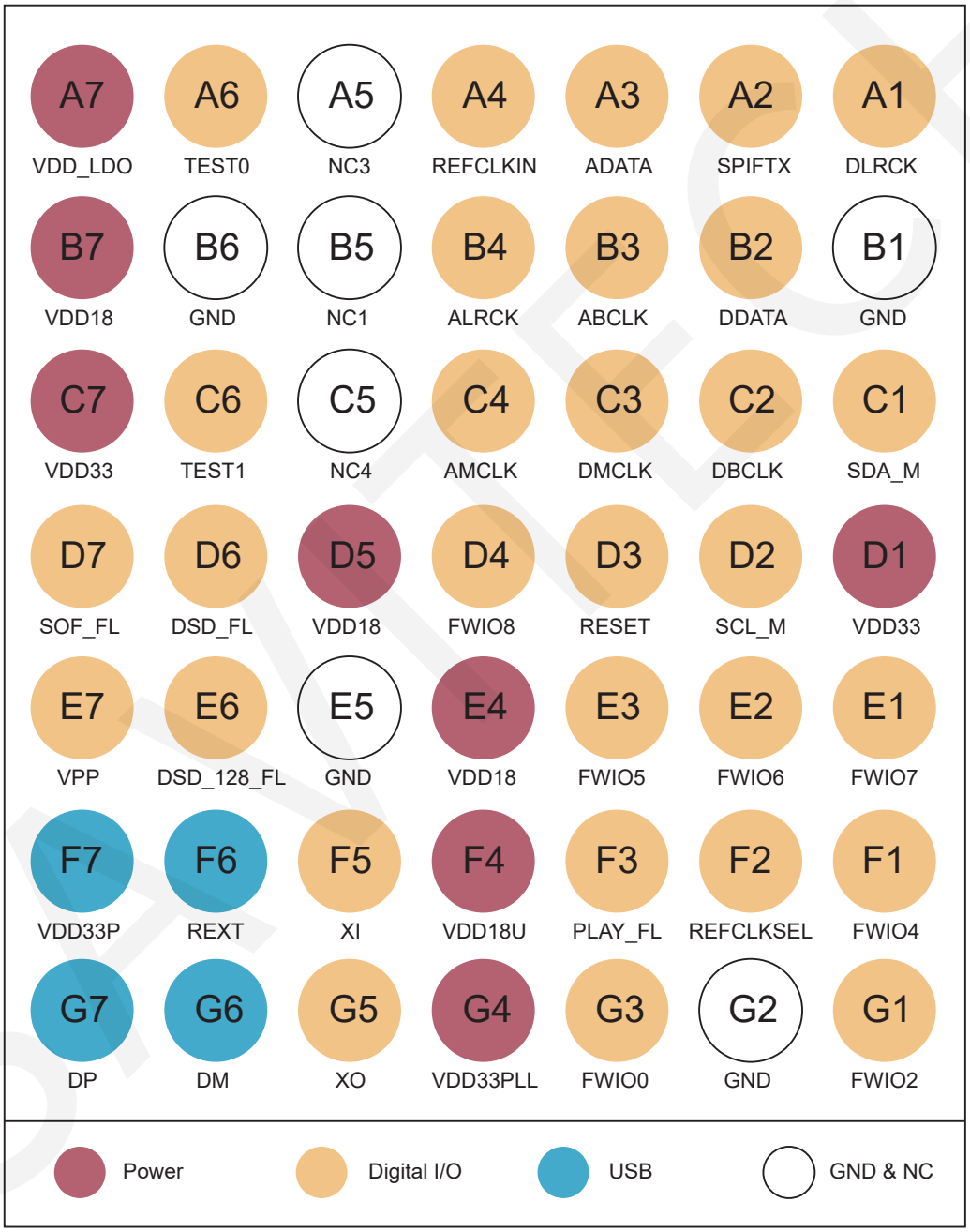


Figure 5-1. WLCSP Pin Diagram (Ball Side Up)

5.2 Pin Functions

PIN		TYPE	DESCRIPTION
NAME	CSP		
VDD_LDO	A7	Power	LDO 3.3V input
VDD18	B7	Power	Connect to 1.8V or connect 1uF capacitor to GND
SOF_FLAG	D7	O	USB Start-Of-Frame indicator
DSD_FLAG	D6	O	DSD/PCM indicator
DSD_128_FLAG	E6	O	DSD64/DSD128 indicator
VPP	E7	Power	OTP Programming Power (Normal Floating)
PLAY_FLAG	F3	OD	Playback indicator
REXT	F6	I	Connect 270ohm resistor to ground
VDD33P	F7	Power	USB2.0 PHY 3.3V power
VDD18U	F4	Power	USB2.0 PHY 1.8V power
GND	E5	Power	USB2.0 PHY ground
DP	G7	I/O	USB2.0 signals
DM	G6	I/O	USB2.0 signals
XI	F5	I	12MHz X'stal input
XO	G5	O	12MHz X'stal output
FWIO0	G3	OD	Firmware assign function I/O port*1
FWIO2	G1	OD	Firmware assign function I/O port*1
FWIO4	F1	OD	Firmware assign function I/O port*1
FWIO5	E3	OD	Firmware assign function I/O port*1
FWIO6	E2	OD	Firmware assign function I/O port*1
FWIO7	E1	OD	Firmware assign function I/O port*1
FWIO8	D4	OD	Firmware assign function I/O port*1
RESET	D3	I	Power-on reset signal (Active low)
SCL_M	D2	O	Master I2C clock
SDA_M	C1	I/O	Master I2C data
DMCLK	C3	I/O	I2S MCLK

DBCLK/DSD_CLK	C2	I/O	I2S BCLK / DSD_CLK
DLRCK/DSD_LEFT	A1	I/O	I2S LRCLK / DSD_LEFT
DDATA/DSD_RIGHT	B2	O	I2S DATA / DSD_RIGHT
SPDIFTX	A2	O	S/PDIF TX output
AMCLK	C4	I/O	I2S MCLK
ABCLK	B3	I/O	I2S BCLK
ALRCK	B4	I/O	I2S LRCK
ADATA	A3	I	I2S DATA
REFCLKIN	A4	I	External reference clock input
REFCLKSEL	F2	OD	External reference clock select
NC1	B5	I	Normal Operation. Needs pull-high
NC3	A5	I	Normal Operation. Needs pull-low
NC4	C5	I	Normal Operation. Needs pull-low
TEST0	A6	I	Normal Operation. Needs pull-low
TEST1	C6	I	Normal Operation. Needs pull-low
VDD33	C7	Power	3.3V Power
VDD33	D1	Power	3.3V Power
VDD33PLL	G4	Power	3.3V PLL Power
VDD18	D5	Power	1.8V Core power
VDD18	E4	Power	1.8V Core power
GND	B1	Power	Ground
GND	B6	Power	Ground
GND	G2	Power	Ground

*1. All FWIOs are firmware assign function input/output, contact FAE to customize.

6. Specifications

6.1 DC Characteristics

Test Conditions: Ta = 25°C; VDD33 = +3.0 ~ +3.6V; fs = 48 kHz-32bit sine wave

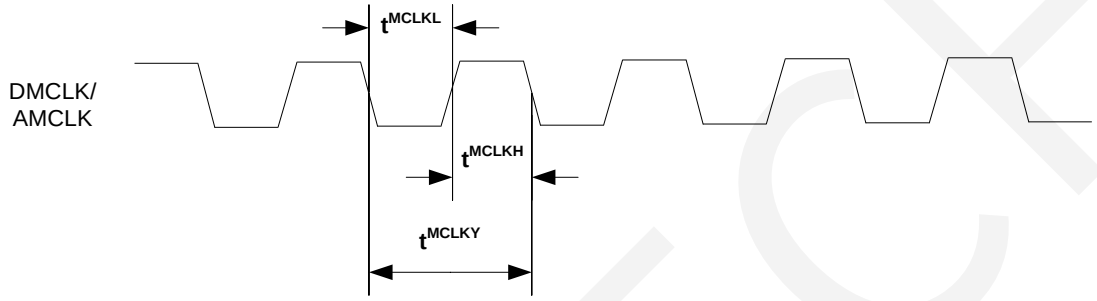
			MIN	MAX	UNIT
Input Low Voltage	VIL	VDD33 = 3.3V		0.3*VDD33	V
Input High Voltage	VIH	VDD33 = 3.3V	0.7*VDD33		V
Output Low Voltage	VOL	IOL = 2mA		0.2	V
Output High Voltage	VOH	IOH =---2mA	VDD33---0.2		V
Input Low Leakage Current	IIL	VIN = 0V VDD33 = 3.6V	---10	10	uA
Input High Leakage Current	IIH	VIN = 3.6V VDD33 = 3.6V	---10	10	uA
Operation Current	Idle*1	VDD33 = 3.3V VDD18 = Ext. DC-DC		30	mA
Operation Current	Up to 192KHz Playback*1	VDD33 = 3.3V VDD18 = Ext. DC-DC		45	mA
Operation Current	Up to 384KHz & DSD Playback*2	VDD33 = 3.3V VDD18 = Ext. DC-DC		66	mA
Suspend Current	Suspend	Total 3.3V rail	2	3	mA
		Total 1.8V rail	2	3	

*1 The power mode is controlled by F/W. This mode can not support DSD.

*2 Support DSD up to DSD128 by DoP and DSD256 by native DSD.

6.2 AC Timing Characteristics

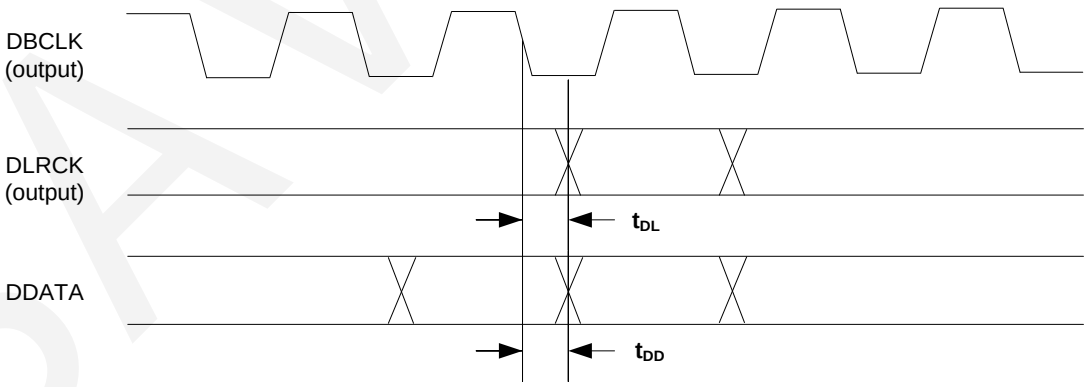
6.2.1 System Clocking Timing



Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24-bit data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DMCLK/AMCLK System clock pulse width high	t^{MCLKL}		41.13		ns
DMCLK/AMCLK System clock pulse width low	t^{MCLKH}		40.23		ns
DMCLK/AMCLK System clock cycle time	t^{MCLKY}		81.36		ns

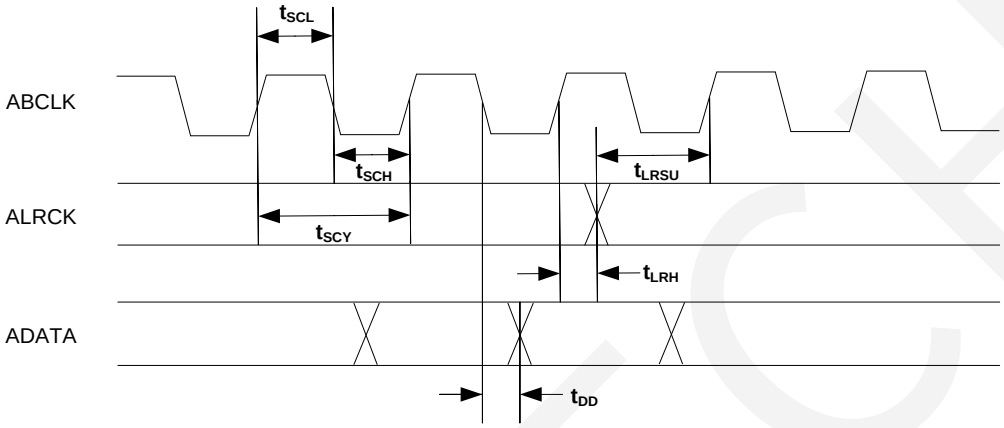
6.2.2 Audio Interface Timing – Master Mode



Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24-bit data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DLRCK propagation delay from DBCLK falling edge	t_{DL}	5			ns
DDATA propagation delay from DBCLK falling edge	t_{DD}	5			ns

6.2.3 Audio Interface Timing – Slave Mode



Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24--bit data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
ABCLK cycle time	t_{SCY}	293	325	358	ns
ALRCK pulse width high	t_{SCH}	144	163	178	ns
ABCLK pulse width low	t_{SCL}	144	163	179	ns
ALRCK set-up time to ABCLK rising edge	t_{LRSU}	10			
ALRCK hold time from ABCLK rising edge	t_{LRH}	10			
ADATA propagation delay from ABCLK falling edge	t_{DD}	5			

6.3 Dynamic Electrical Characteristics (DP/DM)

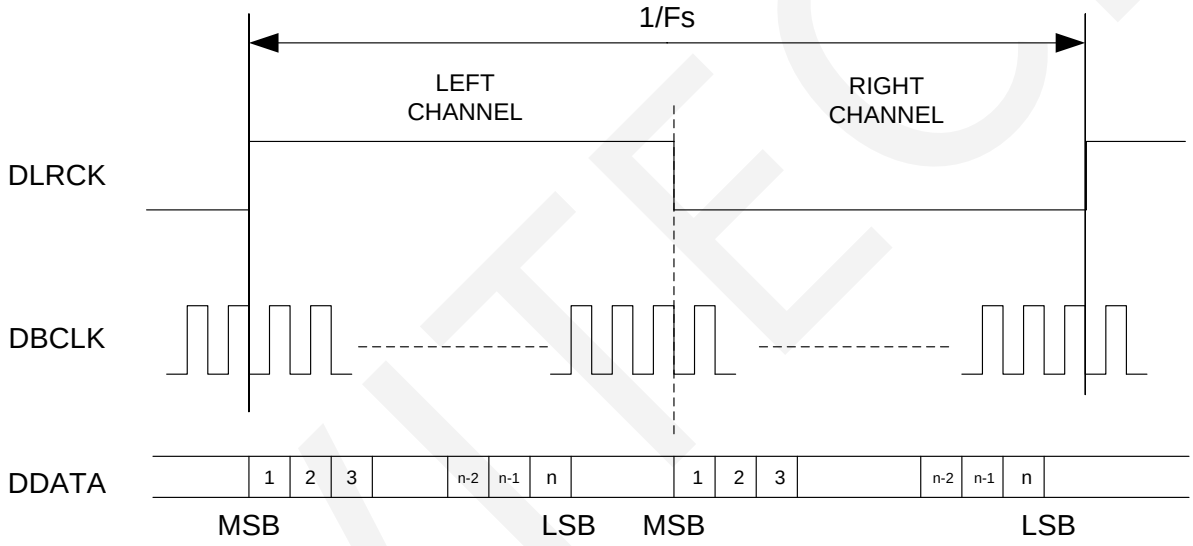
Driver Characteristics:

PARAMETER	SYMBOL	MIN	MAX	UNIT
High – Speed Mode				
High – speed differential rise time (10% - 90%)	t_{HSR}	500		ps
High – speed differential fall time (10% - 90%)	t_{HSF}	500		ps
Full – Speed Mode				
Rise Time for DP/DM	t_{FR}	4	20	ns
Fall Time for DP/DM	t_{FF}	4	20	ns
Differential Rise/Fall Time Matching (t_{FR}/t_{FF})	t_{FRFM}	90	110	%
Output Signal Crossover Voltage	V_{CRS}	1.3	2.0	V

7. Serial Audio Interfaces Formats

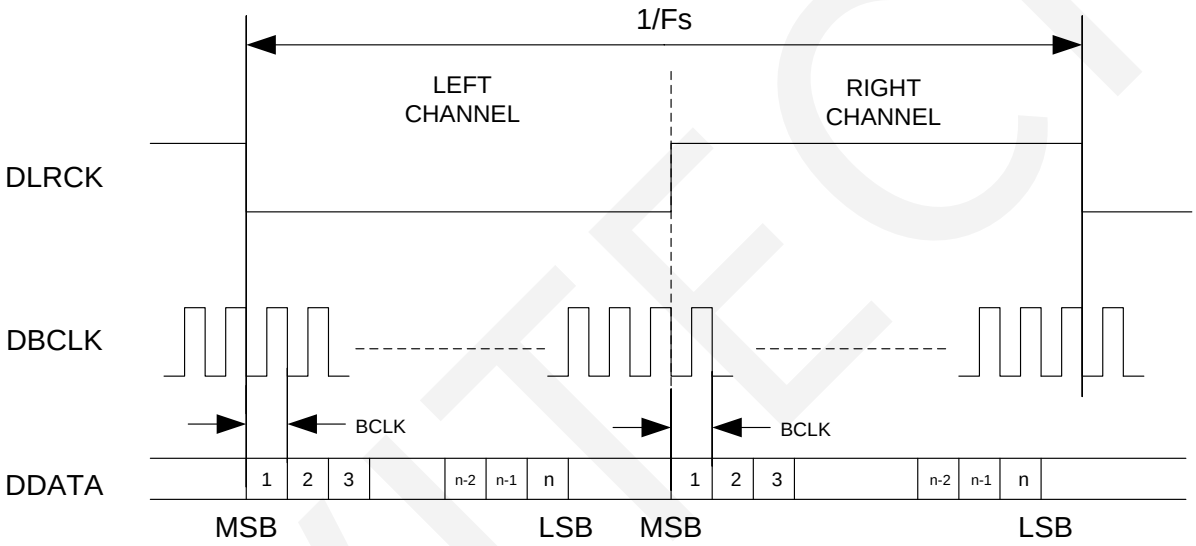
7.1 L - Justified Format

In Left Justified mode, the MSB is available on the first rising edge of DBCLK following an DLRCK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, DBCLK frequency and sample rate, there may be unused DBCLK cycles before each DLRCK transition.



7.2 I2S Format

In I2S mode, the MSB is available on the second rising edge of DBCLK following an DLRCK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, DBCLK frequency and sample rate, there may be unused DBCLK cycles between the LSB of one sample and the MSB of the next.



7.3 Fixed DMCLK Mode

SA9312L supports four different MCLKs during fix mode*1 which can generate high precision clock for DAC/CODEC/ADC.

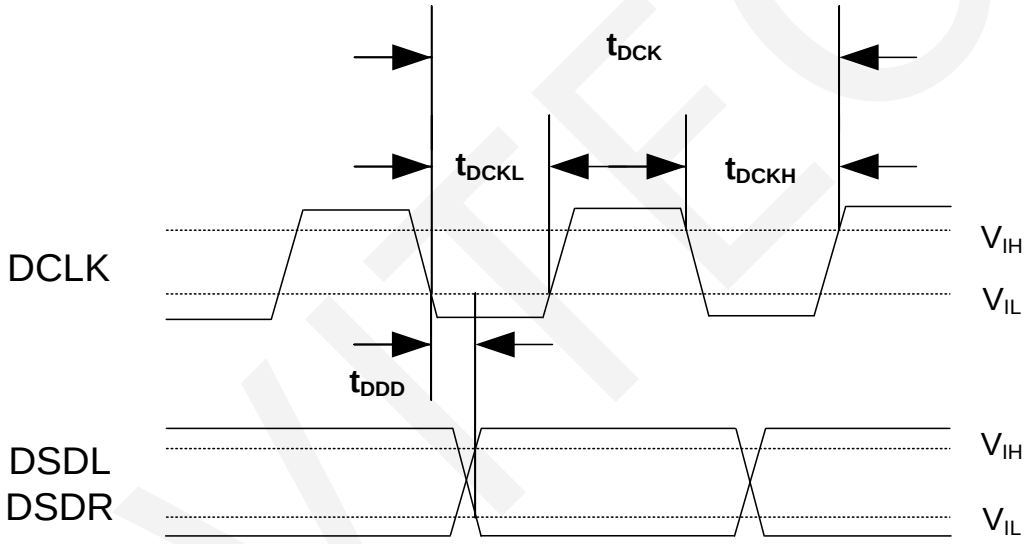
- 11.2896Mhz
- 12Mhz
- 12.288Mhz
- 22.5792Mhz
- 24.576Mhz

*1 The fix mode is controlled by F/W.

8. DSD Audio Data Interfaces

SA9312L supports five modes for playback DSD data over USB Audio stream Supported DSD formats

PARAMETER	SYMBOL	MIN
DSD 64 for 88.2K 32-bit	t_{HSR}	500
DSD 128 for 176.4K 32-bit	t_{HSF}	500
DSD 256 for 352.8K 32-bit	t_{FR}	4
DSD 64 for 176.4K 24-bit	t_{FF}	4
DSD 128 for 352.8K 24-bit	t_{FRFM}	90

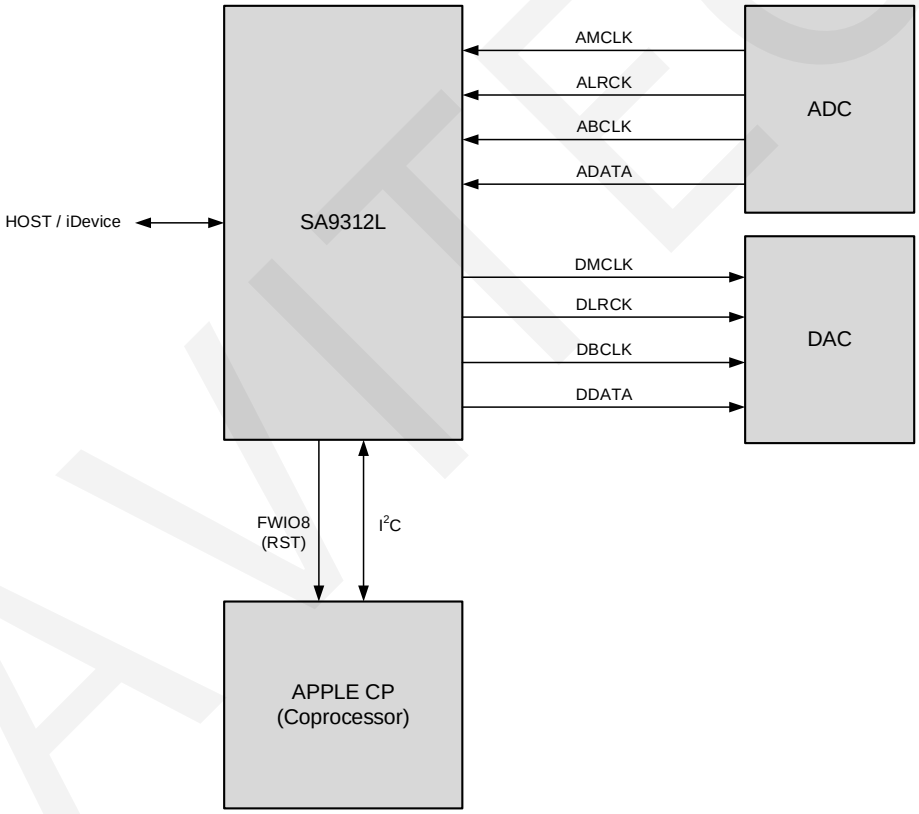


The DSDL and DSDR are all output by negative edge of DCLK. And DSD DAC will sample them by post edge of DCLK.

9. iDevice Support

Apple strongly recommends the use of digital audio paths to and from accessories. Apple device in USB Host Mode audio is the recommended approach. SA9312L will authenticate and identify itself to Apple device using iAP1/iAP2 CP before the iDevice will enumerate and start using USB Audio interface.

- Support 16 /24-bit linear PCM
- Support 44.1 / 48KHz sampling rate and up to 384KHz for future.
- Support input and output audio interface
- Support Volume Control Feature Unit
- Support iAP1 and iAP2 by CP2.0B and CP2.0C.



Digital USB Audio Application For iDevice

10. S/PDIF TX Interfaces

SA9312L support one S/PDIF TX interfaces, each can support up to 24-bit 384K sampling rate. Built in IEC60958 professional S/PDIF TX.

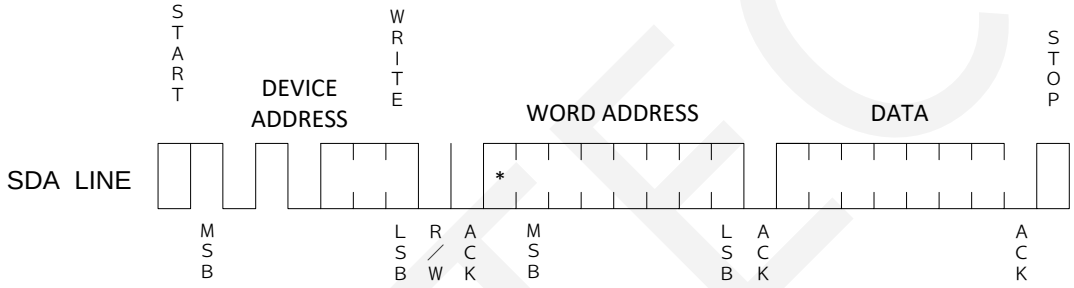
- AES/EBU supported
- DSD stream output on S/PDIF TX
- 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 325.8/ 384KHz sampling rates
- 16/24 bit resolution

11. I²C Master Interfaces

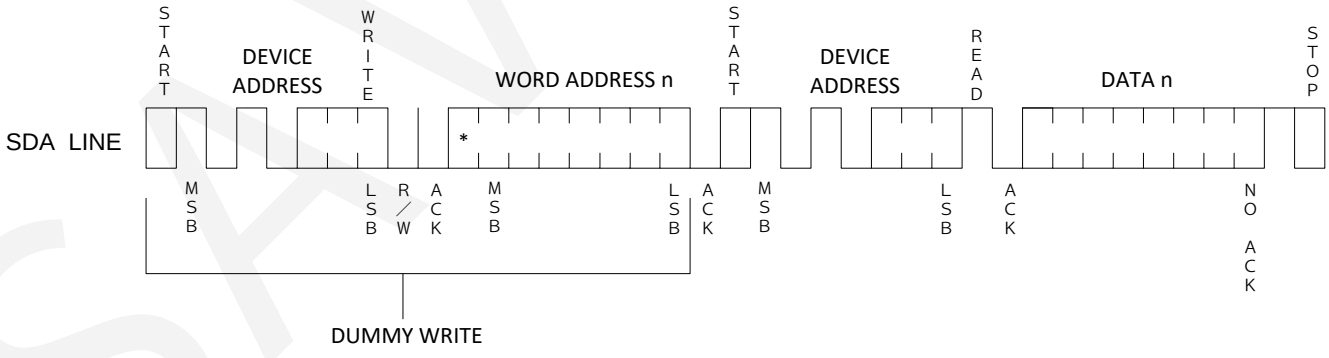
One serial I²C master is supported in SA9312L to control external peripheral devices (EEPROM). SA9312L need an EEPROM to load Firmware code from it.

SA9312L support use I²C Master Interfaces to read/write CP to support Apple MFi.

Byte Write



Random Read



12. Chip Status Flags

SA9312L provide these pins for display chip status flag

FLAGs	Definition
DSD_FLAG	User can check this pin to understand DSD mode is detected or not 0: PCM mode 1: DSD mode
DSD_128_FLAG	User can check this pin to understand which DSD mode is played now (DSD64 or DSD128 mode) 0: DSD 64 mode
USB_HS_FLAG	User can check this pin to understand which USB mode is running now 0: Full Speed 1: High Speed
PLAY_FLAG	User can check this pin to understand which playback status 0: Stop 1: Play

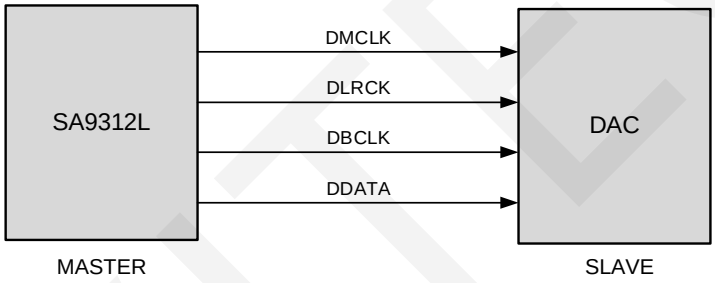
13. Application and Implementation

13.1 Typical Application

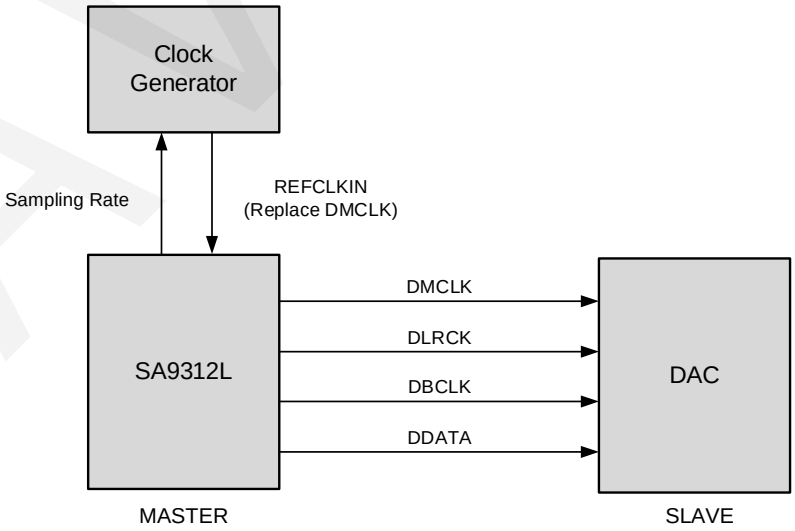
Typical application for SA9312L connecting with DAC / ADC. The following section shows how the SA9312L works with different serial data format including PCM & DSD.

13.1.1 Serial Audio Interfaces Configuration-DAC (Master Mode)

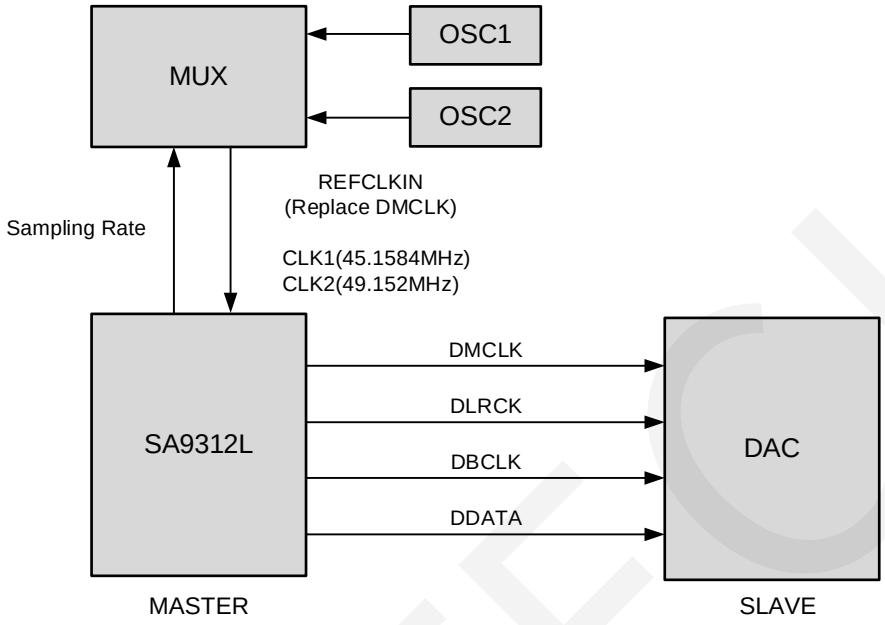
SA9312L supports master mode for following configuration



SA9312L I²S Mater Mode Connection



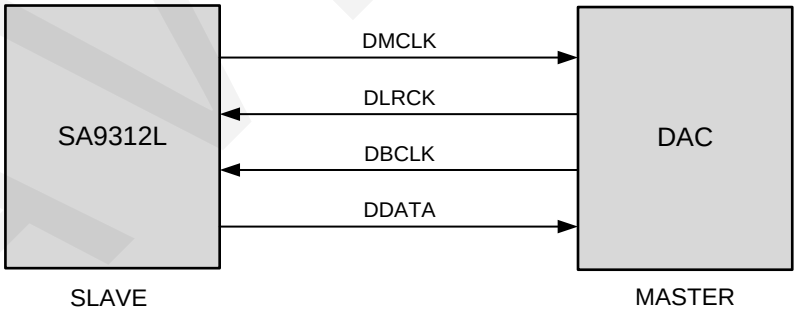
Master Mode (with external REFCLKIN), Mode 0



Master Mode (with external REFCLKIN), Mode 1

13.1.2 Serial Audio Interfaces Configuration-DAC (Slave Mode)

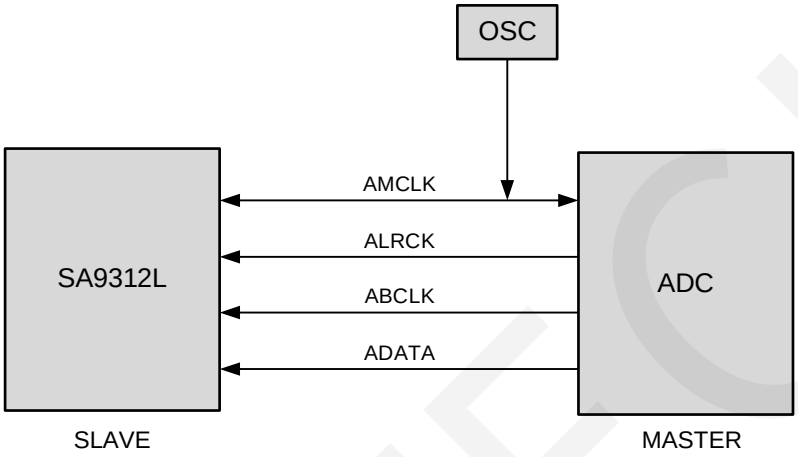
SA9312L supports slave mode for following configuration



SA9312L I²S Slave Mode Connection

13.1.3 Serial Audio Interfaces Configuration-ADC

SA9312L supports slave mode for following configuration



SA9312L I²S Slave Mode Connection

13.1.4 DSD External Control Signals

- DSD_FLAG : (0 : RESET, 1: Normal Operation in DSD format):

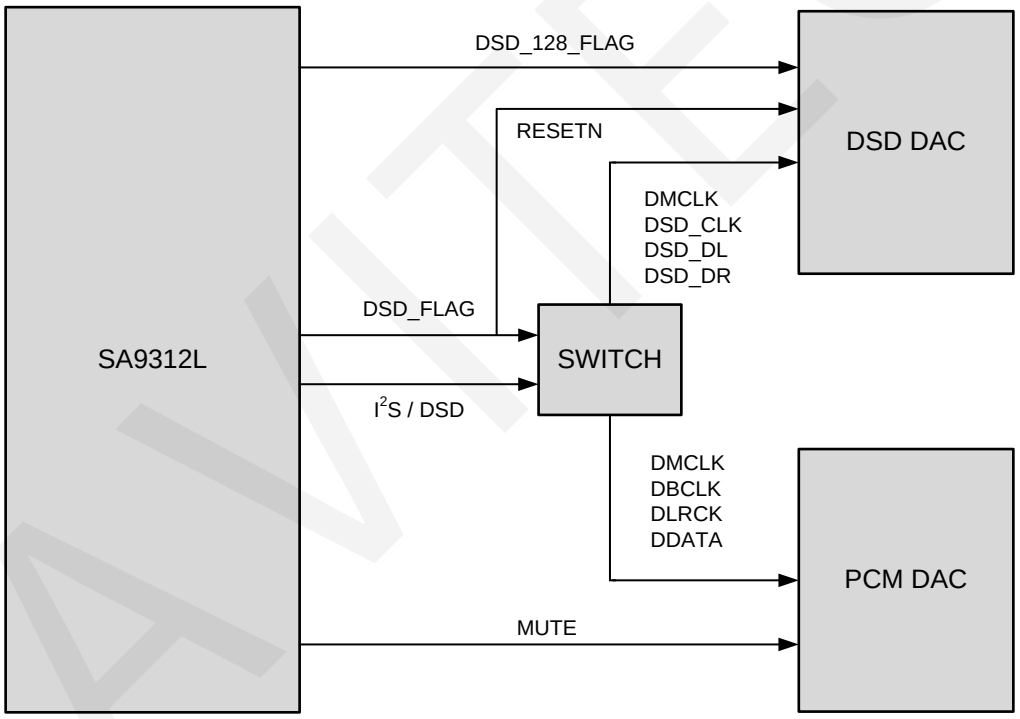
  Used to RESETN DSD DAC.

- DSD_FLAG : (0 : in PCM mode, 1: in DSD mode):

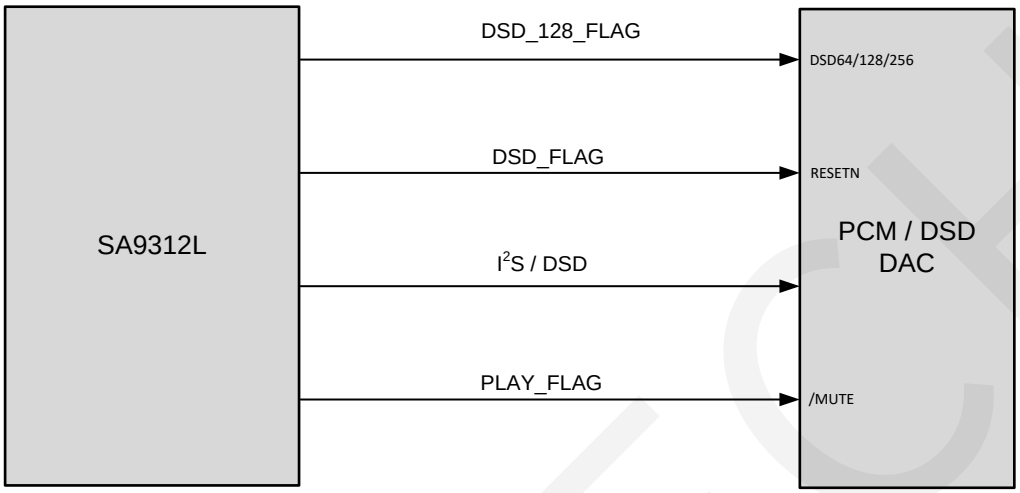
  Used to witch DSD or PCM DAC.

- DSD_128 : (0 : in DSD 64 mode, 1: in DSD 128 mode):

  Used to switch DSD64 and DSD128 format for DSD DAC

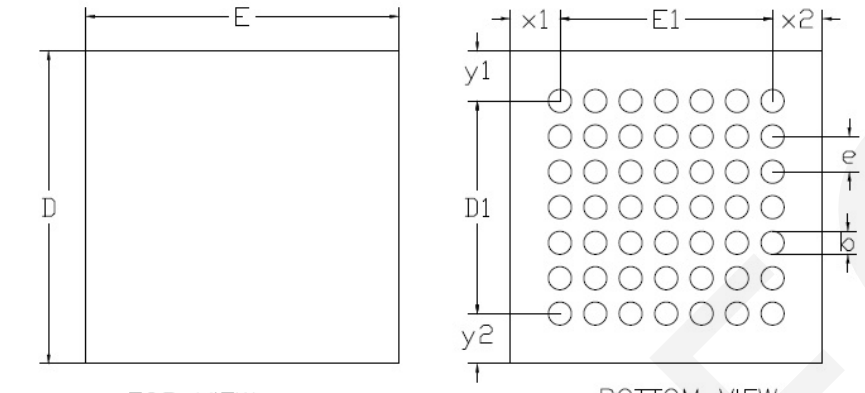


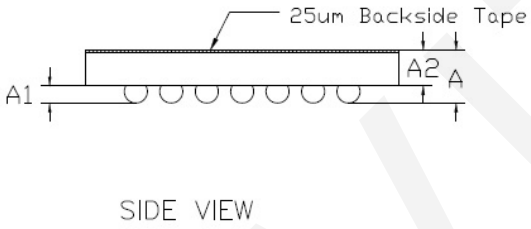
Application with PCM DAC And DSD DAC



Application with PCM/DSD Multi Function DAC

14. Package Outline (WLCSP)





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.540	0.600	0.660
A1	0.165	0.195	0.225
A2	0.380	0.405	0.430
D	3.510	3.530	3.550
D1	2.400BSC		
E	3.510	3.530	3.550
E1	2.400BSC		
b	0.230	0.260	0.290
e	0.400BSC		
x1	0.565 REF		
x2	0.565 REF		
y1	0.565 REF		
y2	0.565 REF		