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BRAVO-DSD
SA9227A

Stereo In/Out
DSD64/ DSD128/DSD256
PCM 32Bit/ 384KHz
USB Audio Streaming Controller

Datasheet v1.3

SAVITECH Corporation

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BRAVO-DSD/PCM
SA9227A
USB Audio Streaming Controller

Overview

The SA9227A is a high performance up to 32bit, 384KHz PCM and DSD64/128/256 streaming USB High-Speed compliant audio steaming controller. It features one stereo playback and recording pairs and one IEC60958 S/PDIF receive and transmit streaming pair. The SA9227A is ideal for both one stereo-in and one stereo-out professional digital audio interface applications. Its PCM resolution and sampling rate can be configurable with 16/24/32 bit and 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384KHz respectively.

Features

- USB 2.0 High-Speed Compliant
- USB Audio Class v1.0 and v2.0 supported
- Incredible Bravo sound quality supported by Savitech innovative Bravo Tech*1
  - Bravo Tech*1 supporting Jitter-less outputs using local clock in Async-mode
- Isochronous input and output endpoints for recording and playback
- One interrupt endpoint for HID
- One DSD interface for connect with external DSD DAC
- Support DSD64 / DSD128 / DSD256 of native and DoP64 / DoP128 in Async mode
- Support DSD L/R data line swap feature
- Support resolutions up to 32-bit and sampling rates up to 384KHz
- Two I2S input pairs and two I2S output pairs for PCM
  - Independent sample rates for each pairs
  - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384 KHz sampling rates
  - 16/24/32 bit resolution
- Built in IEC60958 professional S/PDIF TX and S/PDIF RX,
  - AES/EBU supported
  - SCMS for copyright supported
  - Stereo SPDIF Input and S/PDIF Output
  - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 352.8/ 384 KHz sampling rates
  - 16/24 bit resolution
  - DSD with S/PDIF TX
- Control and I/O
  - I2C bus
  - GPIOs
- 64-pin LQFP packages

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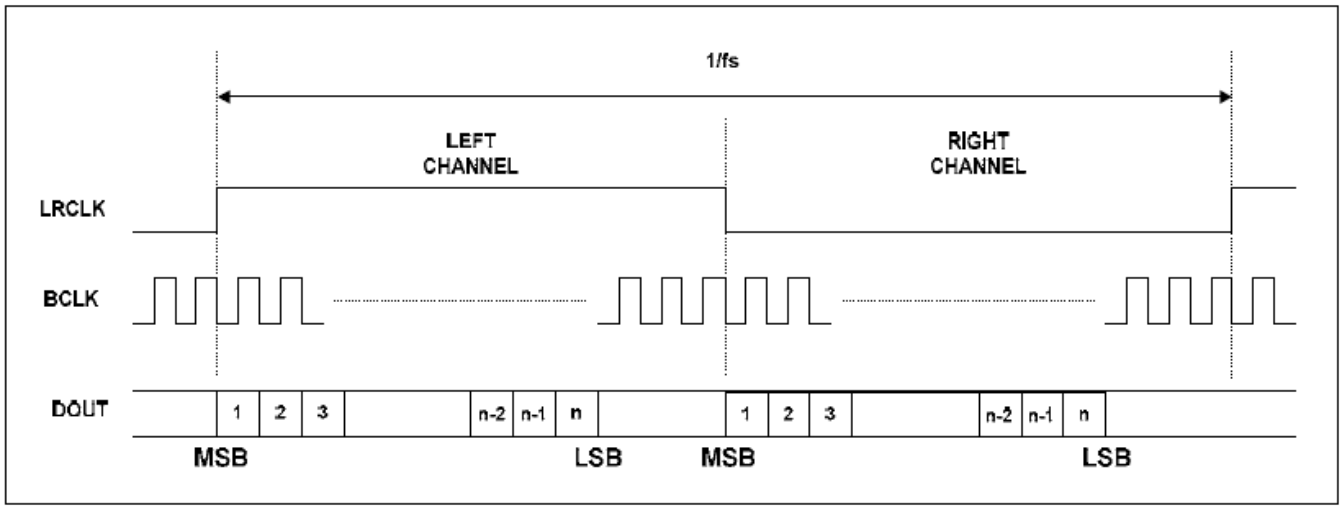
Serial Audio Interfaces Formats

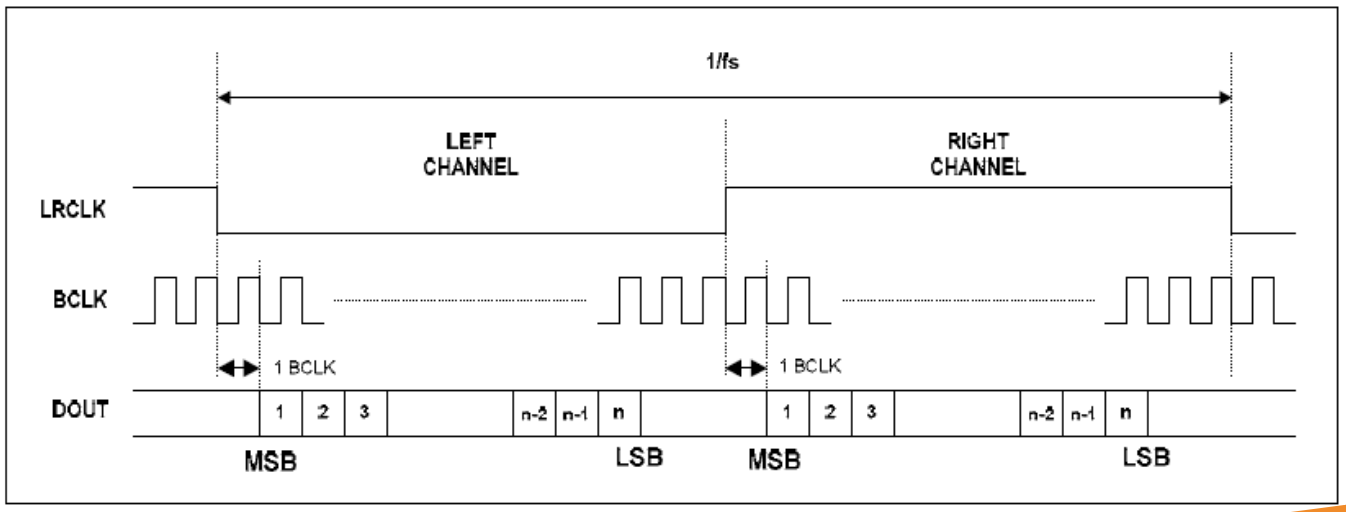
■ L-justified format:

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.



■ I2S format

In I2S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.



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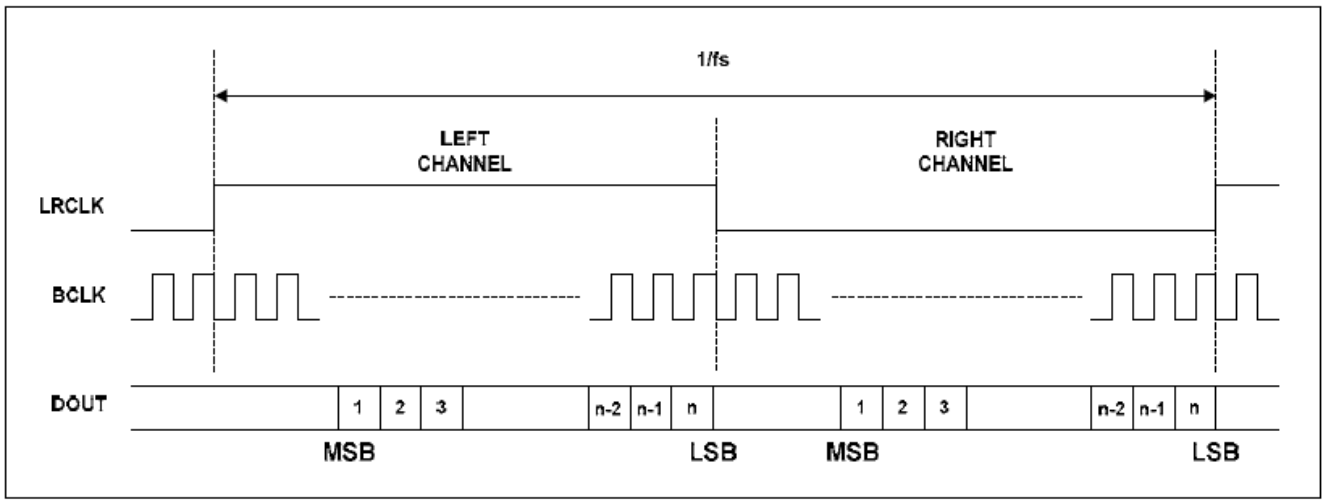
■ R-justified format

In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition. In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.



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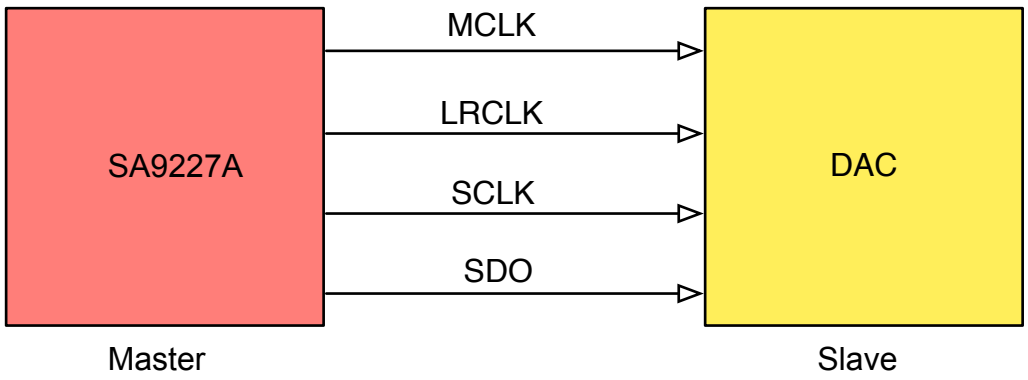
Serial Audio Interfaces Configuration-DAC

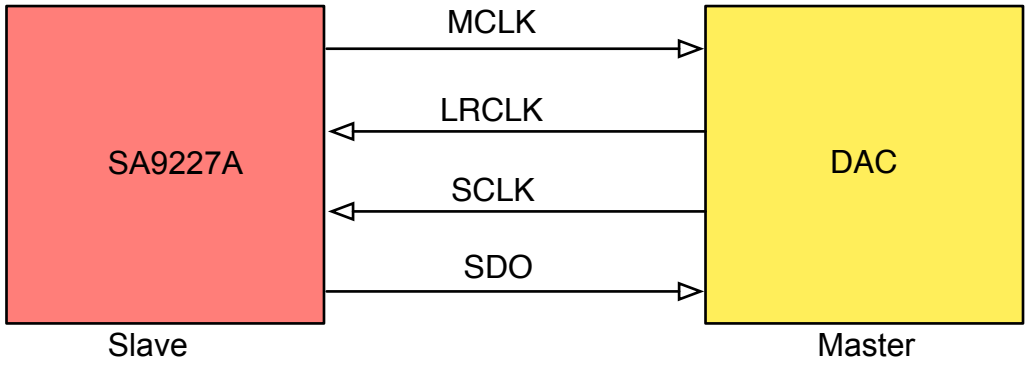
■ SA9227A supports both master mode and slave mode for following configurations.

■ **Master Mode**



SA9227A I2S Master Mode connection

■ **Slave Mode**



SA9227A I2S Slave Mode connection

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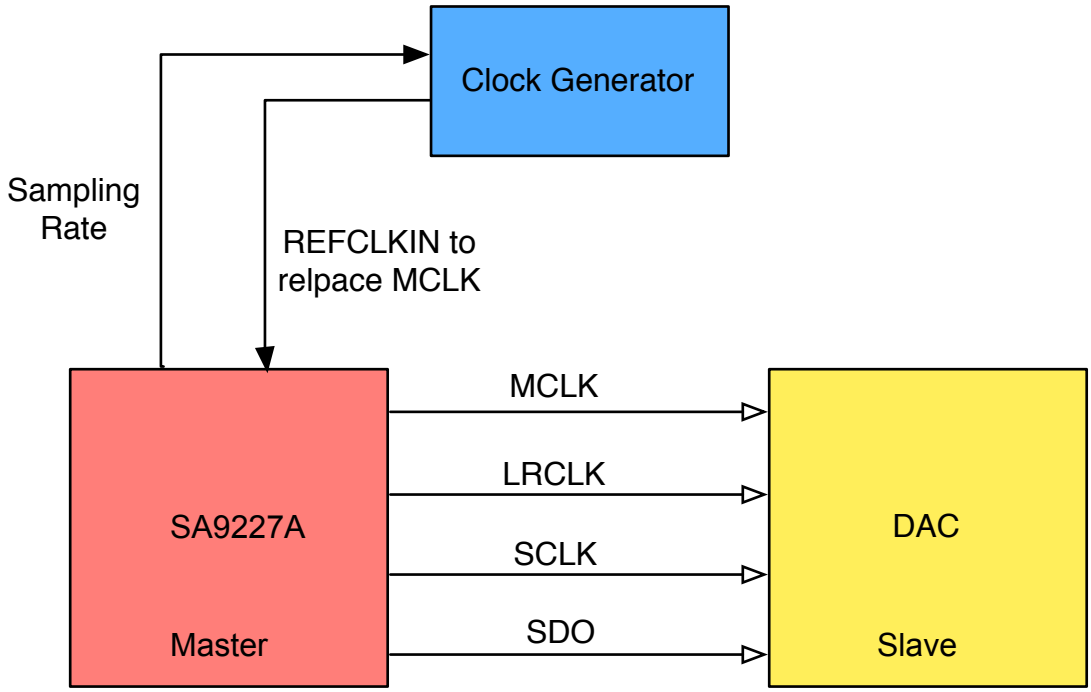
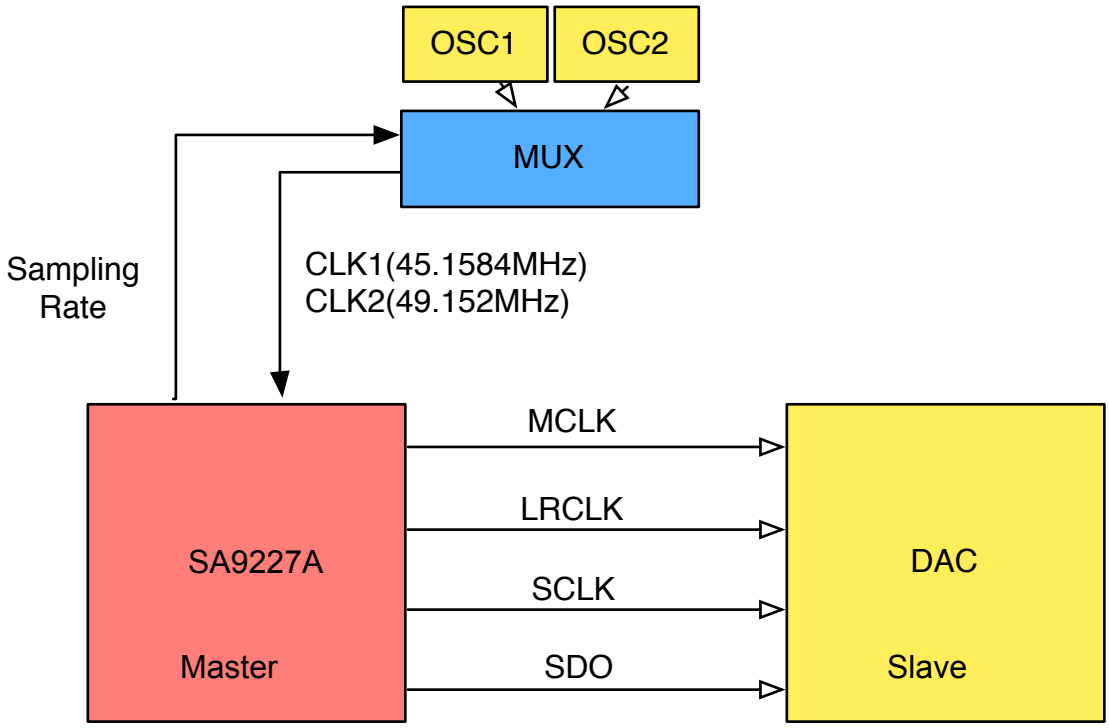
Serial Audio Interfaces Configuration-DAC



Master Mode (with external REFCLKIN), Mode 0



Master Mode (with external REFCLKIN), Mode 1

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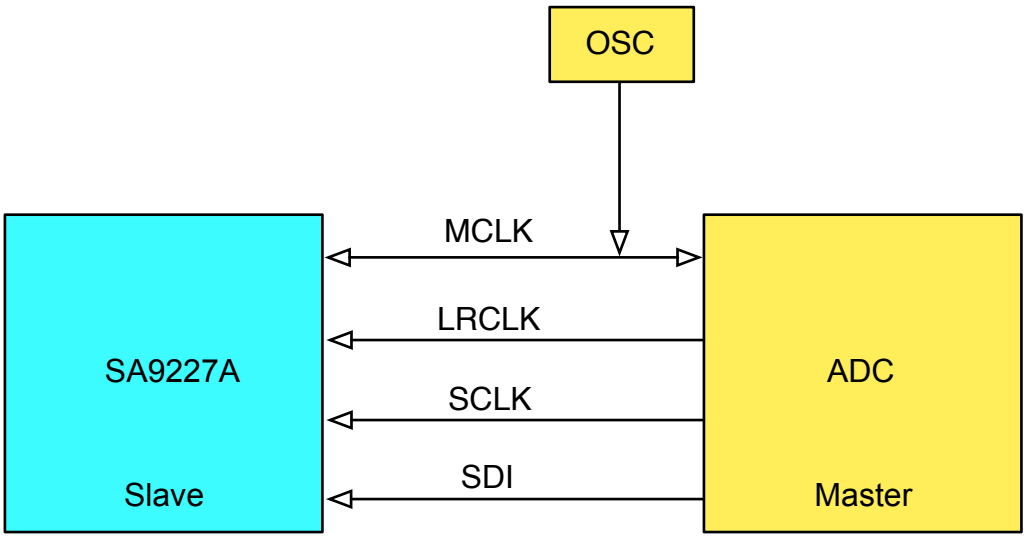
Serial Audio Interfaces Configuration-ADC



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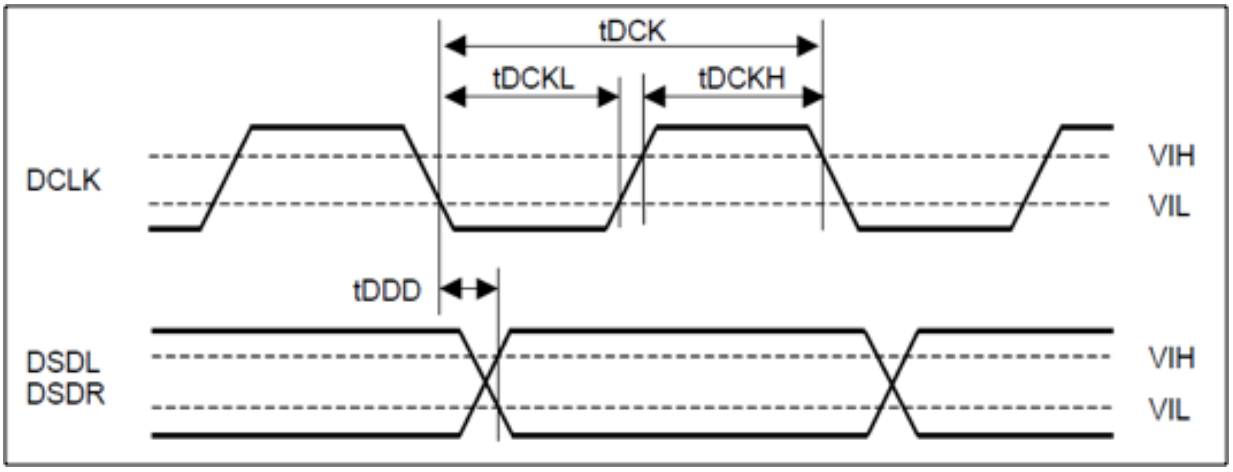
DSD Audio Data Interfaces

Playback:

SA9227A supports five modes for playback DSD data over USB Audio stream

Supported DSD formats:

- DSD 64 for 88.2K 32-bit DCLK(@2.8224MHz) Direct-DSD
- DSD 128 for 176.4K 32-bit DCLK(@5.6448MHz) Direct-DSD
- DSD 256 for 352.8K 32-bit DCLK(@11.2896MHz) Direct-DSD
- DSD 64 for 176.4K 24-bit DCLK(@5.6448MHz) DoP/dCS
- DSD 128 for 352.8K 24-bit DCLK(@11.2896MHz) DoP/dCS



The DSDL and DSDR are all output by negative edge of DCLK. And DSD DAC will sample them by post edge of DCLK.

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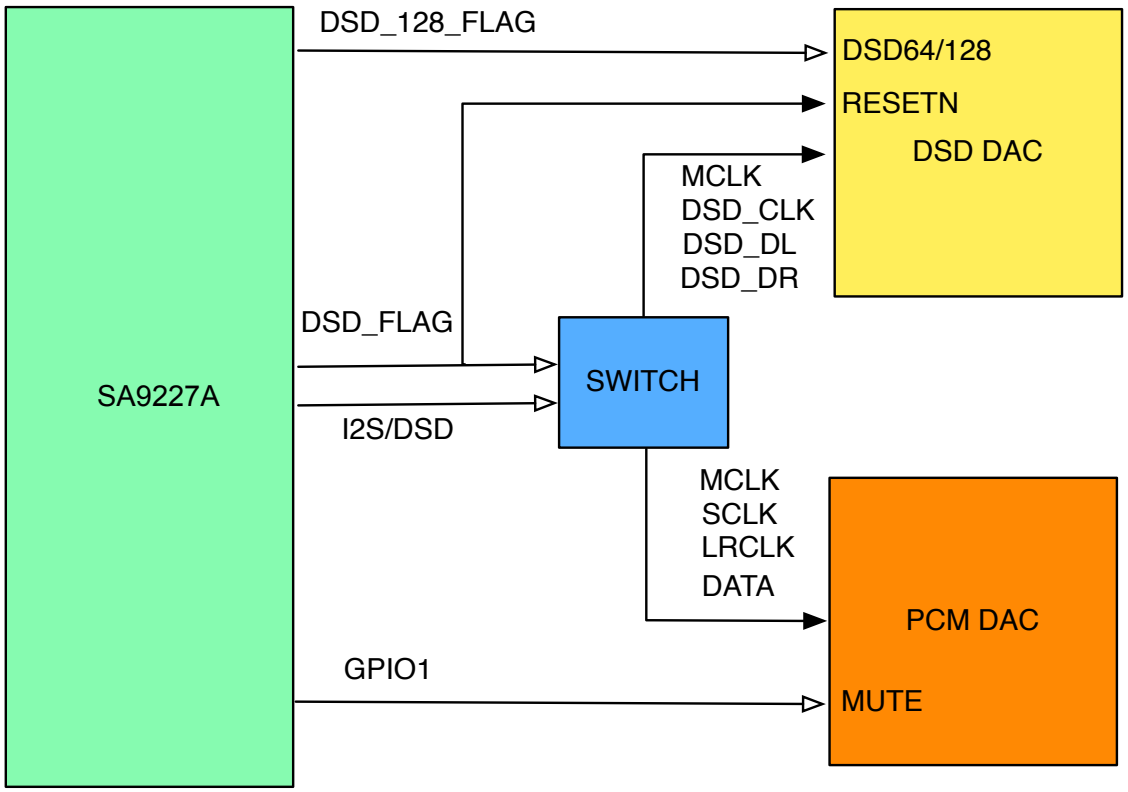
DSD External Control Signals

- DSD_FLAG : (0 : RESET, 1: Normal Operation in DSD format):
  Used to RESETN DSD DAC.

- DSD_FLAG : (0 : in PCM mode, 1: in DSD mode):
  used to switch DSD or PCM DAC.

- DSD_128 : (0 : in DSD 64 mode, 1: in DSD 128 mode):
  used to switch DSD64 and DSD128 format for DSD DAC.



Application with PCM DAC and DSD DAC

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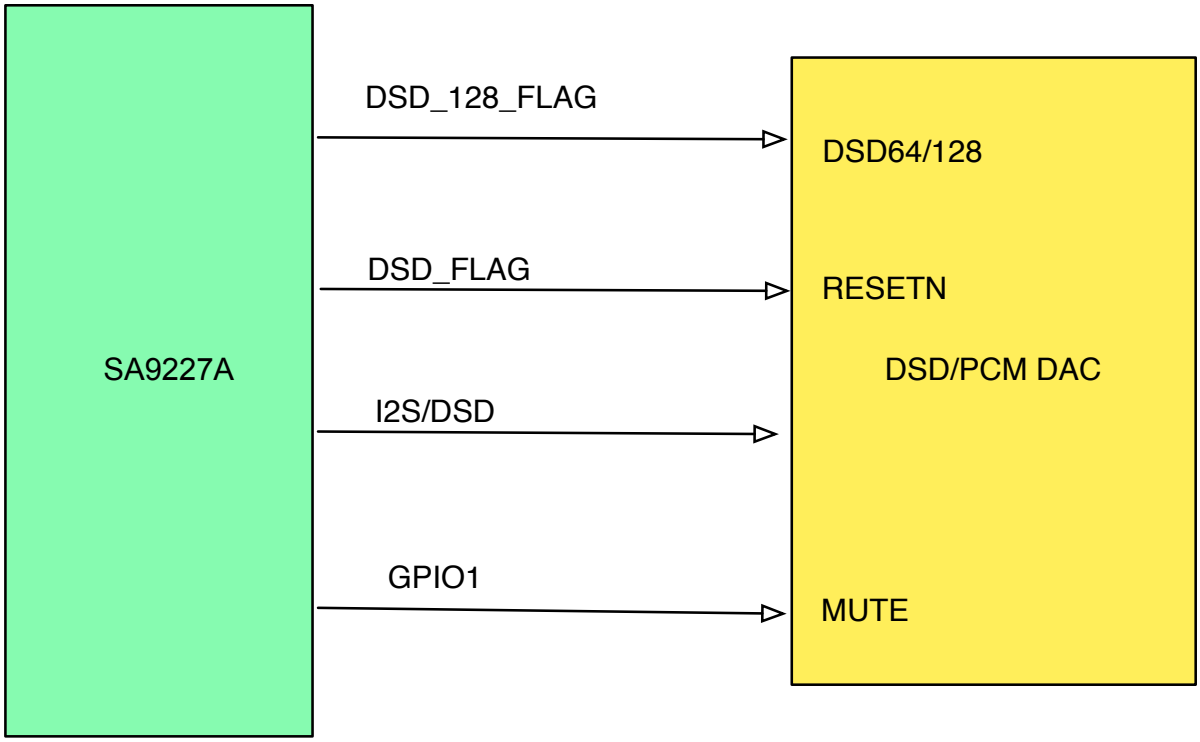

Application with PCM/DSD multi function DAC

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S/PDIF TX & RX Interfaces

SA9227A support one S/PDIF TX and one S/PDIF RX interfaces, each can support up to 24-bit 384K sampling rate. Built in IEC60958 professional S/PDIF TX and SPDIF RX,

- AES/EBU supported
- DSD stream output on S/PDIF TX
- 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192/ 325.8/ 384KHz sampling rates
- 16/24 bit resolution

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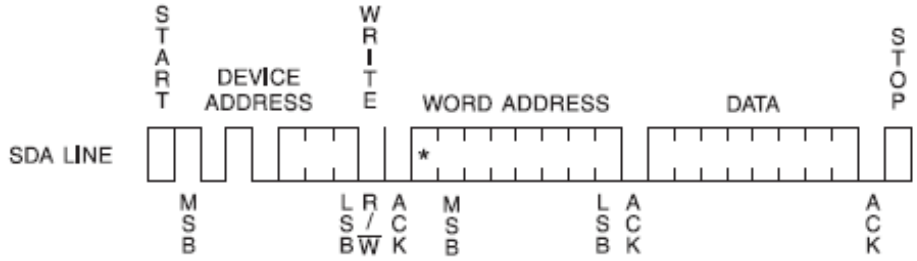
I²C Master Interfaces

One serial I²C master is supported in SA9227A to control external peripheral devices (EEPROM). SA9227A need an EEPROM to load Firmware code from it.

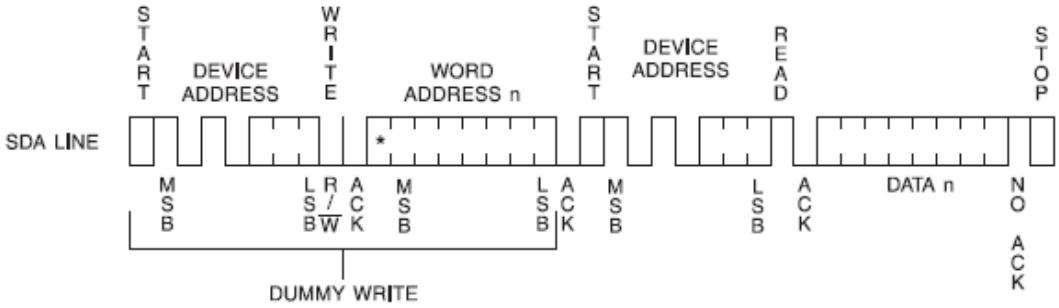
I²C Slave Interfaces

SA9227A have an I2C slave interface which is used for external uC to read status of SA9227A. I2C supports burst read /burst write.

Byte Write



Random Read



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Read Back Registers

Slave I2C Device Address : 0xD5 (I2C Read)

0x10	Flags	Description
	[4] Asynchronous / Adaptive	1 : Asynchronous mode. 0 : Adaptive mode.
	[3] USB High-Speed / Full-Speed	1 : High-Speed. 0 : Full-Speed.
	[2] DSD128	1 : DSD128. 0 : None.
	[1] DSD	1 : DSD. 0 : None.
	[0] SOF	1 : SOF Exist. 0 : SOF Non-Exist.

0x11	Playback Sample Rate	Description
	[6:0] Sample Rate	0x38 384KHz 0x78 352.8KHz 0x18 192KHz 0x58 176.4KHz 0x08 96KHz 0x48 88.2KHz 0x00 48KHz 0x40 44.1KHz 0x0A 32KHz

0x12	Playback bits per sample	Description
	[6:4]	001 16 bits 011 24 bits 111 32 bits

0x13	Mute	Description
	[0] Mute	1 : Enable 0 : Disable

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0x1B	SPDIF Rx Locked Status	Description
	[4]	0 : Unlock 1 : Lock

0x1C	SPDIF Rx Lock Sampling Rate	Description
	[7:0] Sample Rate	0xE8 ~ 0xEC : 32K 0xA8 ~ 0xAB : 44.1K 0x9A ~ 0x9D :48K 0x54 ~ 0x55 : 88.2K 0x4D ~ 0x4E : 96K 0x2A : 176.4K 0x26 ~ 0x27 : 192K 0x15 : 352.8K 0x13 : 384K

0x1D	PLAYBACK FIFO Received Data	Description
	[0]	0 : NO Received Data 1 : Received Data

0x1E	DSD Status	Description
	[6]	0 : No Native DSD 1 : Native DSD 256
	[5]	0 : No Native DSD 1 : Native DSD 128
	[4]	0 : No Native DSD 1 : Native DSD 64
	[1]	0 : No DoP DSD 1 : DoP DSD
	[0]	0 : No Native DSD 1 : Native DSD

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0x50	SPDIF TX channel status Byte0	Description
	[7:0] SPDIF TX channel status Byte0	SPDIF TX channel status Byte0

0x51	SPDIF TX channel status Byte1	Description
	[7:0] SPDIF TX channel status Byte1	SPDIF TX channel status Byte1

0x52	SPDIF TX channel status Byte2	Description
	[7:0] SPDIF TX channel status Byte2	SPDIF TX channel status Byte2

0x53	SPDIF TX channel status Byte3	Description
	[7:0] SPDIF TX channel status Byte3	SPDIF TX channel status Byte3

0x54	SPDIF TX channel status Byte4	Description
	[7:0] SPDIF TX channel status Byte4	SPDIF TX channel status Byte4

0x55	SPDIF TX channel status Byte5	Description
	[7:0] SPDIF TX channel status Byte5	SPDIF TX channel status Byte5

0x56	SPDIF TX channel status Byte6	Description
	[7:0] SPDIF TX channel status Byte6	SPDIF TX channel status Byte6

0x57	SPDIF TX channel status Byte7	Description
	[7:0] SPDIF TX channel status Byte7	SPDIF TX channel status Byte7

0x58	SPDIF TX channel status Byte8	Description
	[7:0] SPDIF TX channel status Byte8	SPDIF TX channel status Byte8

0x59	SPDIF TX channel status Byte9	Description
	[7:0] SPDIF TX channel status Byte9	SPDIF TX channel status Byte9

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General Purpose Interface IN /OUT

Eight GPIOs pins are supported that can be controlled by standard USB HID requests.

GPIOs	**Definition** **Playback only**	**Definition** **Playback and recording**
GPIO1	Use for reset DAC	
GPIO2	High/Full speed selector, “1”: Full-speed, “0”: High-speed	
	Selection of 49MHz, 45MHz external clocks for reference input pin (57 pin), ‘0’: 49Mhz, ‘1’:45MHz	
GPIO6 GPIO5 GPIO4 GPIO3	GPIO[6:5:4:3] 0010: 32KHz 0001: 44.1KHz 0000: 48KHz 1101: 88.1KHz 1100: 96KHz 1011: 176.4KHz 1010: 192KHz 1001: 352.8KHz 1000: 384KHz	
GPIO8	Used for CP reset	

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DSD External Control Signals

SA9227A provide these pins for DSD and special usage

FLAGs	Definition
SOF_FLAG	User can check this pin to understand USB is in suspend or not 0: USB is in suspend 1: USB is in normal mode
DSD_FLAG	User can check this pin to understand DSD mode is detected or not 0: PCM mode 1: DSD mode
DSD_128_FLAG	User can check this pin to understand which DSD mode is played now (DSD64 or DSD128 mode) 0: DSD 64 mode 1: DSD 128 mode

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Pin Assignment

Pin	Name	Pin	Name
1	VDD33_LDO	33	GPIO4
2	GND_LDO	34	GPIO5
3	VDD18_LDO	35	GPIO6
4	VDD33	36	GPIO7
5	GND	37	GPIO8
6	SPDIF_RX	38	RESETN
7	VDD33	39	VDD33
8	VDD18	40	SCL_M
9	SOF_FLAG	41	SDA_M
10	DSD_FLAG	42	DBCLK / DSD_CLK
11	DSD_128_FLAG	43	VDD18
12	REXT	44	VDD33
13	VDD33	45	DDATA / DSD_RIGHT
14	VDD33	46	DMCLK
15	DP	47	DLRCK / DSD_LEFT
16	DM	48	SPDIF_TX
17	GND	49	ABCLK
18	XI	50	ADATA
19	XO	51	AMCLK
20	VDD18	52	VDD33
21	VDD33	53	ALRCK
22	GND	54	SCL_S
23	GND	55	SDA_S
24	VDD33	56	VDD33
25	GND	57	REFCLKIN
26	VDD33	58	VDD18
27	GPIO0	59	TEST1
28	VDD18	60	TEST2
29	VDD33	61	TEST3
30	GPIO1	62	TEST4
31	GPIO2 / USB (HS/FS) SEL	63	TEST5
32	GPIO3	64	TEST6

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Pin Description

Pin	Name	I/O/P	Description
1	VDD33_LDO	P	LDO Input
2	GND_LDO	P	LDO Ground
3	VDD18_LDO	P	LDO Output
4	VDD33	P	SPDIF RX power
5	GND	P	SPDIF RX ground
6	SPDIF_RX	I	S/PDIF RX input
7	VDD33	P	I/O power
8	VDD18	P	Core power
9	SOF_FLAG	O	USB SOF(Start Of Frame) indicator
10	DSD_FLAG	O	DSD/PCM indicator: 0: PCM 1: DSD
11	DSD_128_FLAG	O	DSD64/DSD128 indicator
12	REXT	I	Connect 270ohm resistor to ground
13	VDD33	P	USB2.0 PHY power
14	VDD33	P	USB2.0 PHY power
15	DP	I/O	USB2.0 signals
16	DM	I/O	USB2.0 signals
17	GND	P	USB2.0 PHY ground
18	XI	I	12MHz X'stal
19	XO	O	12MHz X'stal
20	VDD18	P	USB2.0 PHY power
21	VDD33	P	PLL power
22	GND	P	PLL ground
23	GND	P	PLL ground
24	VDD33	P	PLL power
25	GND	P	PLL ground
26	VDD33	P	PLL power
27	GPIO0	OD, I/O	General purpose I/O
28	VDD18	P	Core power
29	VDD33	P	I/O power
30	GPIO1	OD, I/O	For DSD DAC reset
31	GPIO2 / USB (HS/FS) SEL	OD, I/O	HID/ Pull-high for USB Full-speed or pull-low for High-speed select
32	GPIO3	OD, I/O	Audio stream sampling rate indicator 0

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Pin	Name	I/O/P	Description
33	GPIO4	OD, I/O	Audio stream sampling rate indicator 1
34	GPIO5	OD, I/O	Audio stream sampling rate indicator 2
35	GPIO6	OD, I/O	Audio stream sampling rate indicator 3
36	GPIO7	OD, I/O	Audio stream resolution indicator 1
37	GPIO8	OD, I/O	For CP reset
38	RESETN	I	Power-on reset signal (active low)
39	VDD33	P	I/O power
40	SCL_M	I/O	Master I2C clock
41	SDA_M	I/O	Master I2C data
42	DBCLK / DSD_CLK	I/O	I2S output BCLK/ DSD_CLK
43	VDD18	P	Core power
44	VDD33	P	I/O power
45	DDATA / DSD_RIGHT	O	I2S ouput DATA / DSD_RIGHT
46	DMCLK	I/O	I2S output MCLK
47	DLRCK/ DSD_LEFT	I/O	I2S output LRCLK/ DSD_LEFT
48	SPDIF_TX	O	S/PDIF TX output
49	ABCLK	I/O	I2S input BCLK
50	ADATA	I	I2S input DATA
51	AMCLK	I/O	I2S input MCLK
52	VDD33	P	I/O power
53	ALRCK	I/O	I2S input LRCLK
54	SCL_S	I/O	Slave I2C clock
55	SDA_S	I/O	Slave I2C data
56	VDD33	P	I/O power
57	REFCLKIN	I	Optional external reference clock input
58	VDD18	P	Core power
59	TEST1	I	Normal Operation needs pull-high
60	TEST2	I	Normal Operation needs pull-down
61	TEST3	I	Normal Operation needs pull-down
62	TEST4	I	Normal Operation needs pull-down
63	TEST5	I	Normal Operation needs pull-down
64	TEST6	I	Normal Operation needs pull-down

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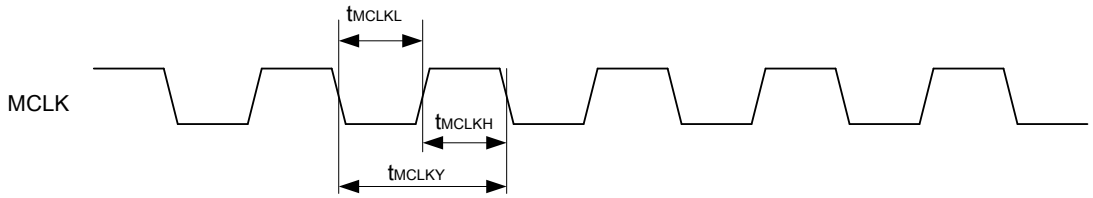
DC Characteristics

Test Conditions: Ta = 25°C; VDD33 = +3.0 ~ +3.6V; fs = 48 kHz-32bit sine wave

Parameter	Symbol	Test Condition	Min.	Max.	Unit
Input Low Voltage	VIL	VD33 = 3.3V		0.3*VDD33	V
Input High Voltage	VIH	VDD33 = 3.3V	0.7*VDD33		V
Output Low Voltage	VOL	IOL = 2mA		0.2	V
Output High Voltage	VOH	IOH = -2mA	VDD33-0.2		V
Input Low Leakage Current	IIL	VIN = 0V VDD33 = 3.6V	-10	10	uA
Input High Leakage Current	IIH	VIN = 3.6V VDD33 = 3.6V	-10	10	uA
Operation Power Current		VDD33 = 3.3V VDD18 = Int. LDO		150	mA
Operation Power Current		VDD33 = 3.3V VDD18 = Ext. DC-DC		104	mA

AC Timing Characteristics

1. System Clock Timing



Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24-bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
MCLK System clock pulse width high	tMCLKL		41.13		ns
MCLK System clock pulse width low	tMCLKH		40.23		ns
MCLK System clock cycle time	tMCLKY		81.36		ns

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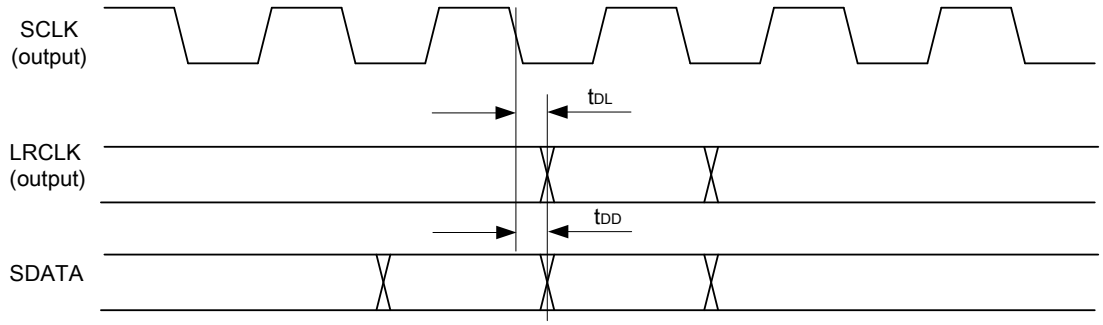
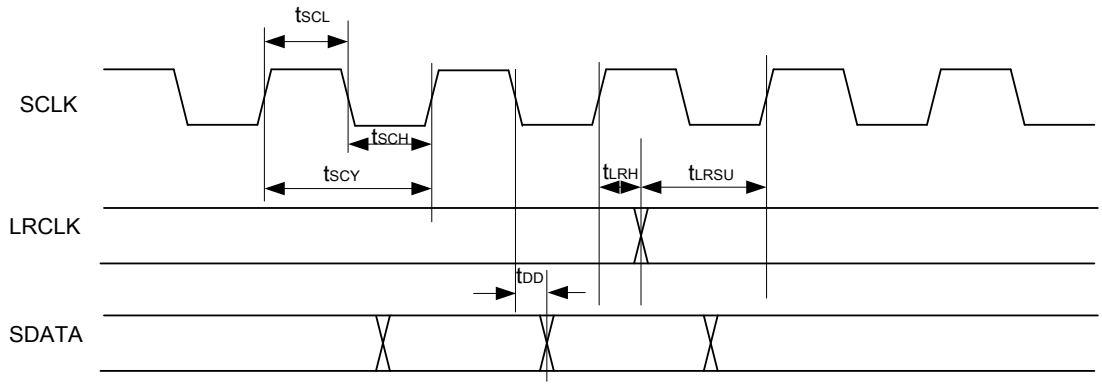
2. Audio Interface Timing – Master Mode



Test Conditions: VDD = V, VSS = 0V, TA = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24-bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
LRCLK propagation delay from SCLK falling edge	tDL	5			ns
SDATA propagation delay from SCLK falling edge	tDDA	5			ns

3. Audio Interface Timing – Slave Mode



Test Conditions: VDD = V, VSS = 0V, TA = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24-bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
SCLK cycle time	tSCY	293	325	358	ns
LRCLK pulse width high	tSCH	144	163	179	ns
SCLK pulse width low	tSCL	144	163	179	ns

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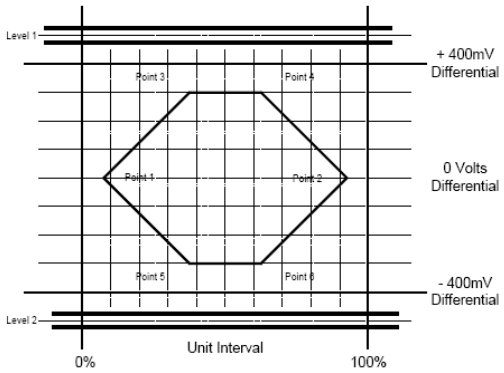
LRCLK set-up time to SCLK rising edge	tLRSU	10			ns
LRCLK hold time from SCLK rising edge	tLRH	10			ns
SDATA propagation delay from SCLK falling edge	tDD	5			ns

Dynamic Electrical Characteristics: (DP/DM)

Driver Characteristics:

Symbol	Parameter	Min	Max	Unit
High-speed Mode				
t_{HSR}	High-speed differential rise time (10% - 90%)	500	-	ps
t_{HSF}	High-speed differential fall time (10% - 90%)	500	-	ps
Full-speed Mode				
t_{FR}	Rise Time for DP/DM	4	20	ns
t_{FF}	Fall Time for DP/DM	4	20	ns
t_{FRFM}	Differential rise/fall Time Matching (t_{FR} / t_{FF})	90	110	%
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V

Driver Timing/Receiver timing:

<table>
<tr><th>Symbol</th><th>Description</th><th>Condition</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th></tr>
<tr><td colspan="7">Driver timing</td></tr>
<tr><td colspan="7">High-speed mode</td></tr>
<tr><td>Driver waveform requirement</td><td colspan="2">See the eye pattern of template 1 (described in the USB 2.0 spec.)
 
</td><td colspan="4">Follow template 1 described in USB specification Rev 2.0.
<table>
<tr><th></th><th>Voltage Level (D+ - D-)</th><th>Time (% of Unit Interval)</th></tr>
<tr><td>Level 1</td><td>525 mV in UI following a transition, 475 mV in all others</td><td>N/A</td></tr>
<tr><td>Level 2</td><td>-525 mV in UI following a transition, -475 in all others</td><td>N/A</td></tr>
<tr><td>Point 1</td><td>0 V</td><td>7.5% UI</td></tr>
<tr><td>Point 2</td><td>0 V</td><td>92.5% UI</td></tr>
<tr><td>Point 3</td><td>300 mV</td><td>37.5% UI</td></tr>
<tr><td>Point 4</td><td>300 mV</td><td>62.5% UI</td></tr>
<tr><td>Point 5</td><td>-300 mV</td><td>37.5% UI</td></tr>
<tr><td>Point 6</td><td>-300 mV</td><td>62.5% UI</td></tr>
</table></td></tr>
<tr><td colspan="7">Full-speed mode</td></tr>
</table>

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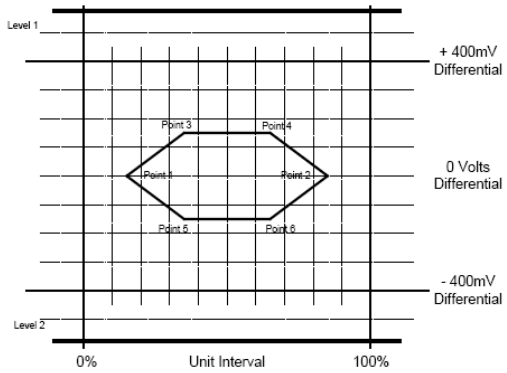
<table>
<tr><td>Propagation delay (VI, FSE 0, OE to DP, DM)</td><td colspan="2">For the detailed description of VI, FSE 0, and OE, (please refer to the USB 1.1 spec.)</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
<tr><td colspan="7">Receiver timing</td></tr>
<tr><td colspan="7">High-speed mode (template 4, USB 2.0 spec.)</td></tr>
<tr><td>Data source jitter and receiver jitter tolerance</td><td colspan="2">See the eye pattern of template 4 (described in the USB 2.0 spec.)
 
</td><td colspan="4">Follow template 4 described in USB specification Rev 2.0.
<table><tr><th></th><th>Voltage Level (D+ - D-)</th><th>Time (% of Unit Interval)</th></tr><tr><td>Level 1</td><td>575 mV</td><td>N/A</td></tr><tr><td>Level 2</td><td>-575 mV</td><td>N/A</td></tr><tr><td>Point 1</td><td>0 V</td><td>15% UI</td></tr><tr><td>Point 2</td><td>0 V</td><td>85% UI</td></tr><tr><td>Point 3</td><td>150 mV</td><td>35% UI</td></tr><tr><td>Point 4</td><td>150 mV</td><td>65% UI</td></tr><tr><td>Point 5</td><td>-150 mV</td><td>35% UI</td></tr><tr><td>Point 6</td><td>-150 mV</td><td>65% UI</td></tr></table></td></tr>
<tr><td colspan="7">Full-speed mode</td></tr>
<tr><td>$t_{PLH(rcv)}$
$t_{PHL(rcv)}$</td><td colspan="2">Receiver propagation delay (DP; DM to RX_RCV)</td><td>For the detailed description of RCV, (please refer to the USB 1.1 spec.)</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
<tr><td>$t_{PLH(single)}$
$t_{PHL(single)}$</td><td colspan="2">Receiver propagation delay (DP; DM to VOP, VON)</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
</table>

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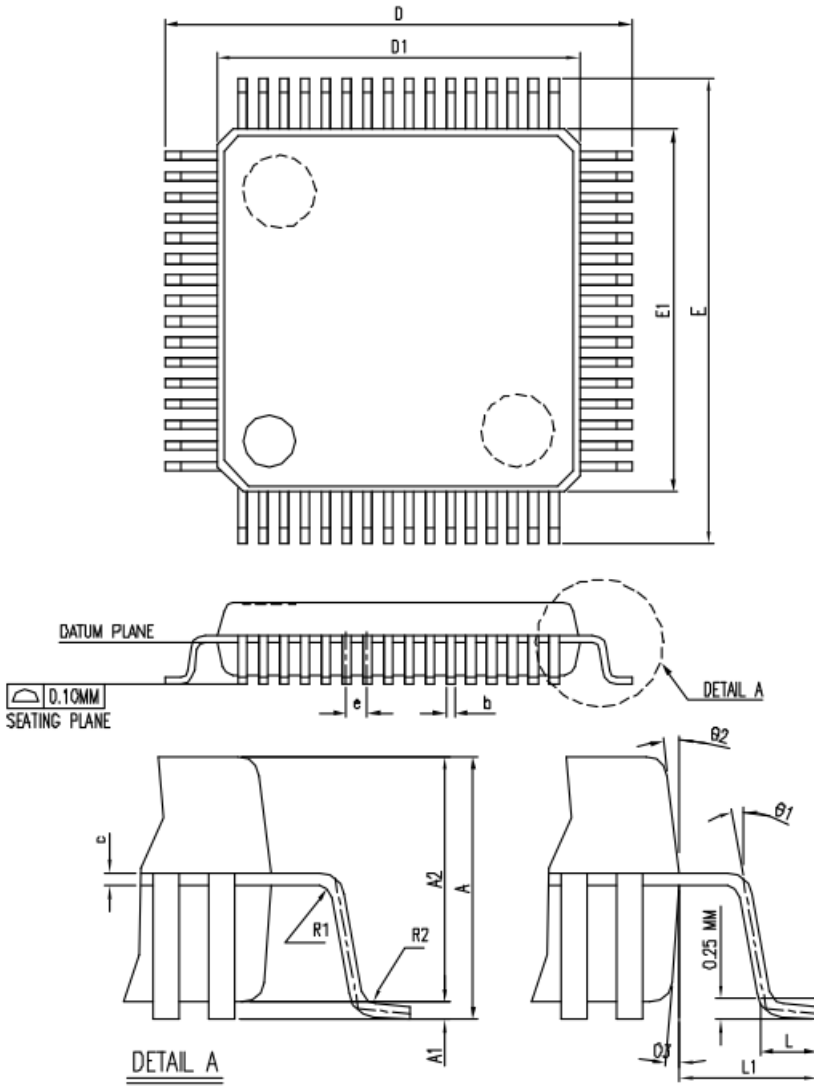
LQFP 64 MECHANICAL DATA



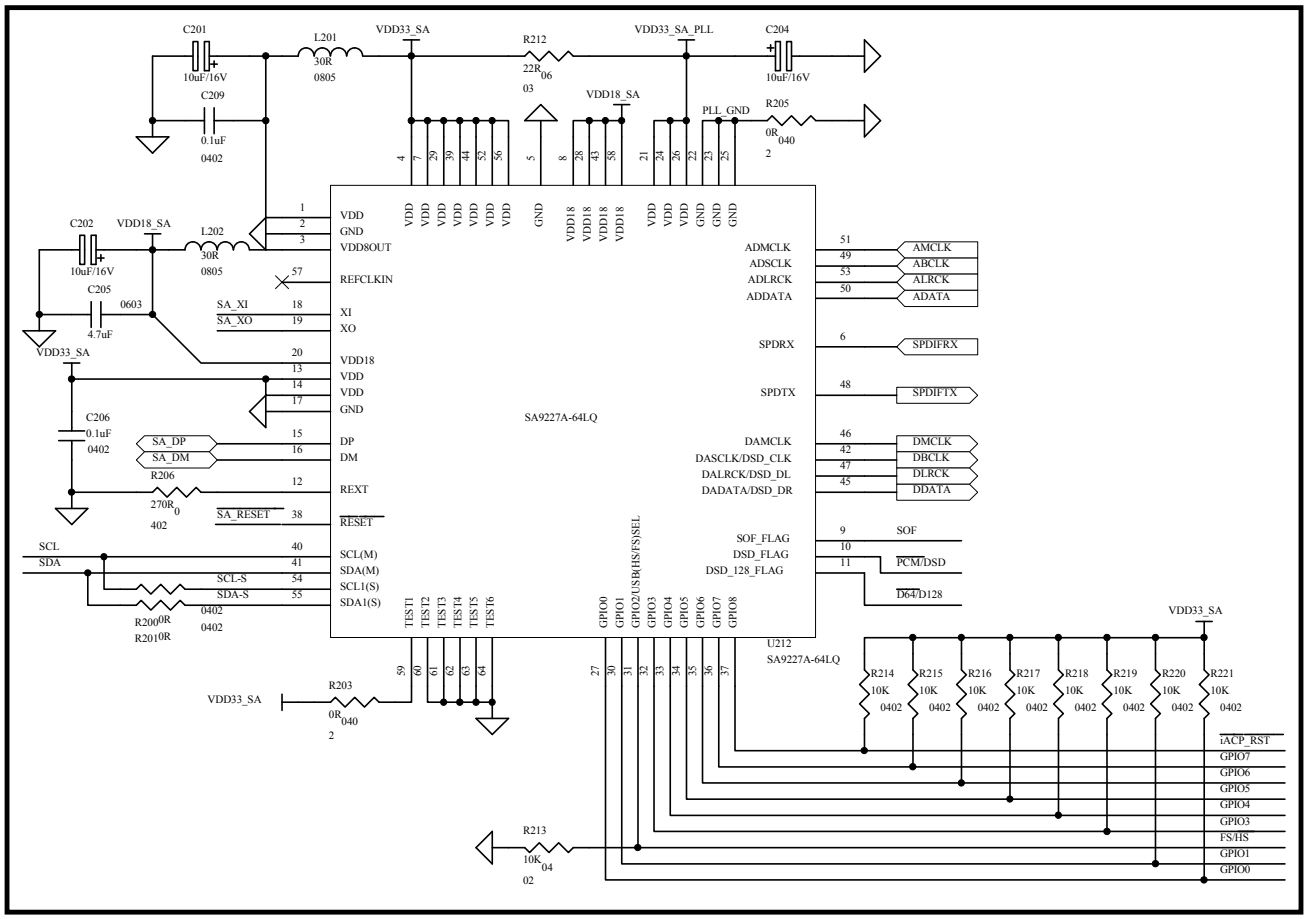
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.0019		0.0059
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09		0.20	0.0035		0.0078
e	0.40 BASIC			0.016 BASIC		
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.0031		
R2	0.08		0.20	0.0031		0.0078
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
JEDEC	MS-026 (BBD)					

*NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

* IC surface marking with abbreviation SA9227

REFERENCE DESIGN

SA9227A-64LQ



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