盛微先進科技
SAVITECH.COM

BRAVO
SA9128

4-Stereo Out
1-Stereo In
PCM 24Bit / 48KHz
USB Audio Streaming Controller

Datasheet v1.0

SAVITECH Corporation

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BRAVO-PCM
SA9128
USB Audio Streaming Controller

Overview

The SA9128 is a USB High-Speed compliant audio steaming controller. It features four stereo playback and one stereo recording pairs and one IEC60958 S/PDIF receiver. The SA9128 is ideal for both one stereo-in and four stereo-out professional digital audio interface applications. Its PCM resolution and sampling rate can be configurable with 24 bit and 32/ 44.1/ 48 KHz respectively.

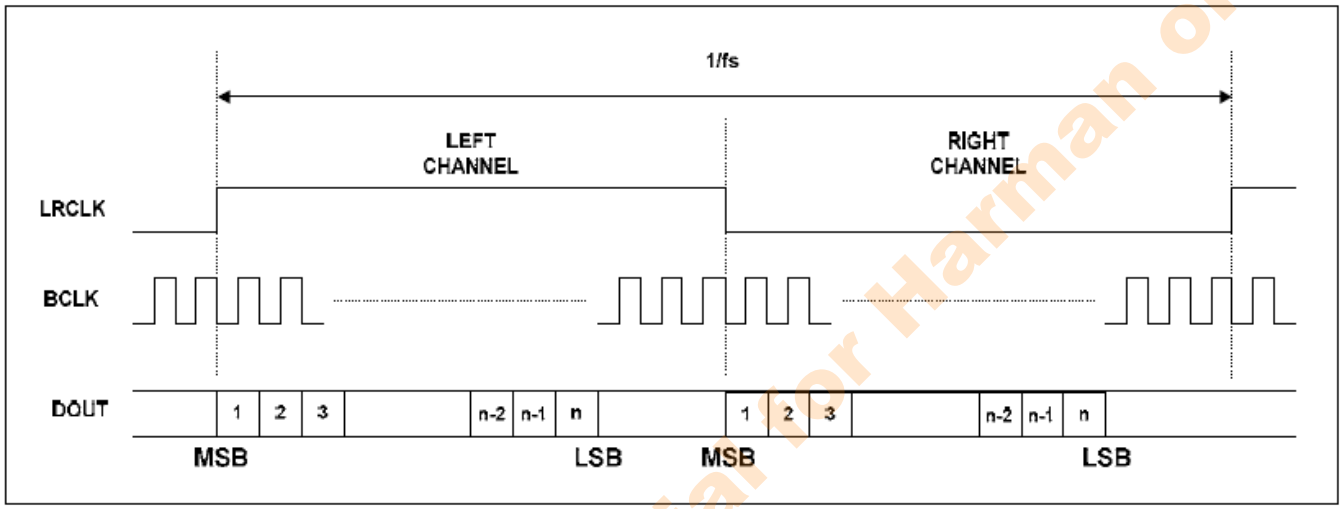
Features

- USB 2.0 High-Speed Compliant
- USB Audio Class v1.0 and v2.0 supported
- Incredible Bravo sound quality supported by Savitech innovative Bravo Tech*1
  - Bravo Tech*1 supporting Jitter-less outputs using local clock in Async-mode
- Isochronous input and output endpoints for recording and playback
- One interrupt endpoint for HID
- Support resolutions up to 24-bit and sampling rates up to 48KHz
- Two I2S input pairs and four I2S output pairs for PCM
  - Independent sample rates for each pairs
  - 32/ 44.1/ 48 KHz sampling rates
  - 24 bit resolution
- Built in IEC60958 professional S/PDIF RX
  - AES/EBU supported
  - SCMS for copyright supported
  - Stereo SPDIF Input
  - 32/ 44.1/ 48 KHz sampling rates
  - 24 bit resolution
- Control and I/O
  - I2C bus
  - SPI
  - GPIOs
- 64-pin TQFP packages

Serial Audio Interfaces Formats

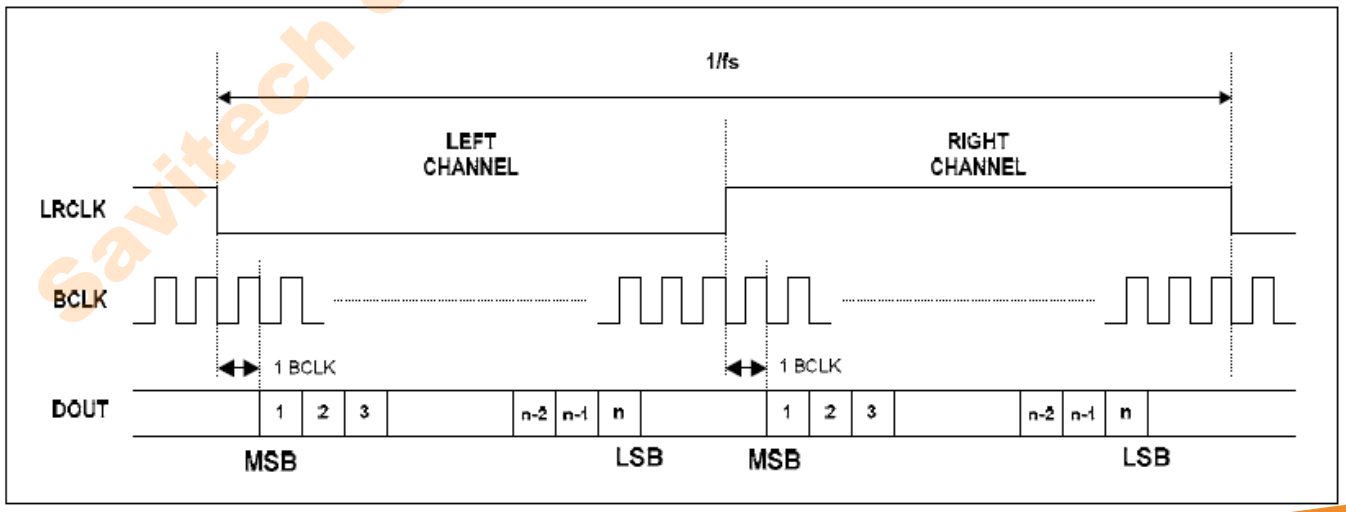
■ L-justified format:

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.



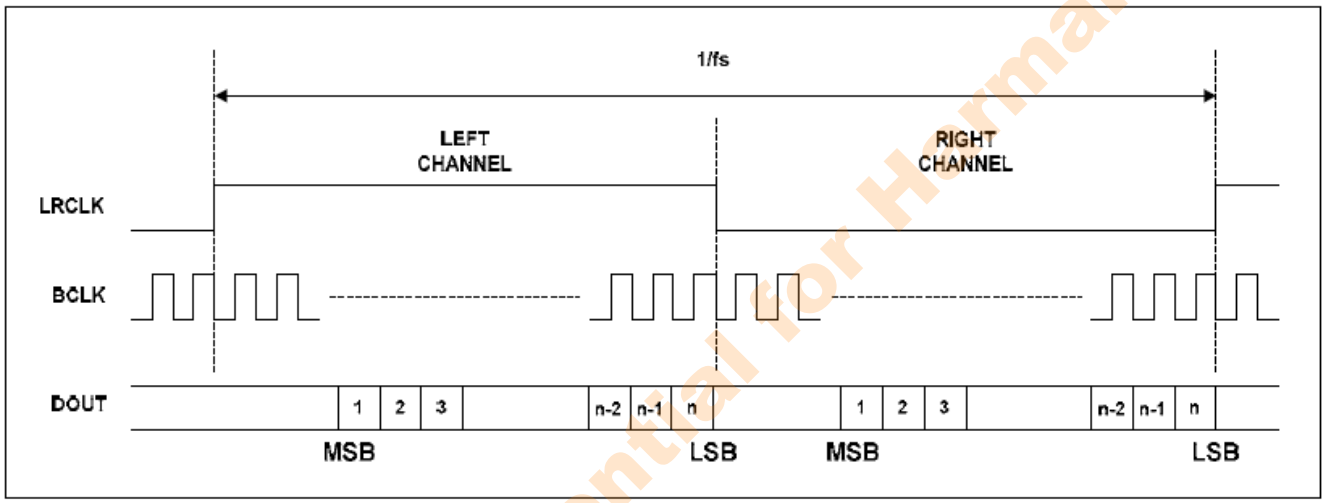
■ I2S format

In I2S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.



■ R-justified format

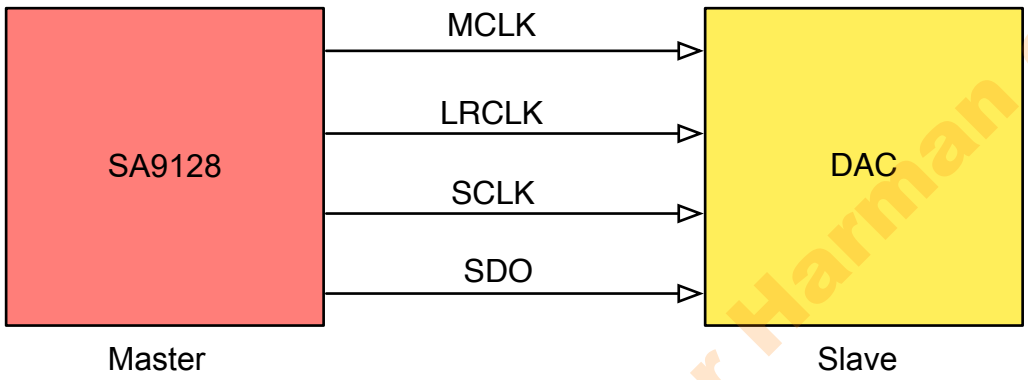
In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition. In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.



Serial Audio Interfaces Configuration-DAC

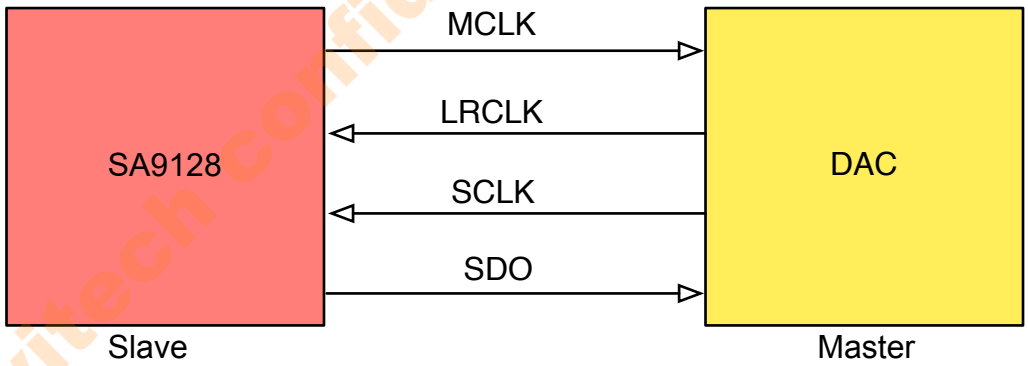
■ SA9128 supports both master mode and slave mode for following configurations.

■ **Master Mode**



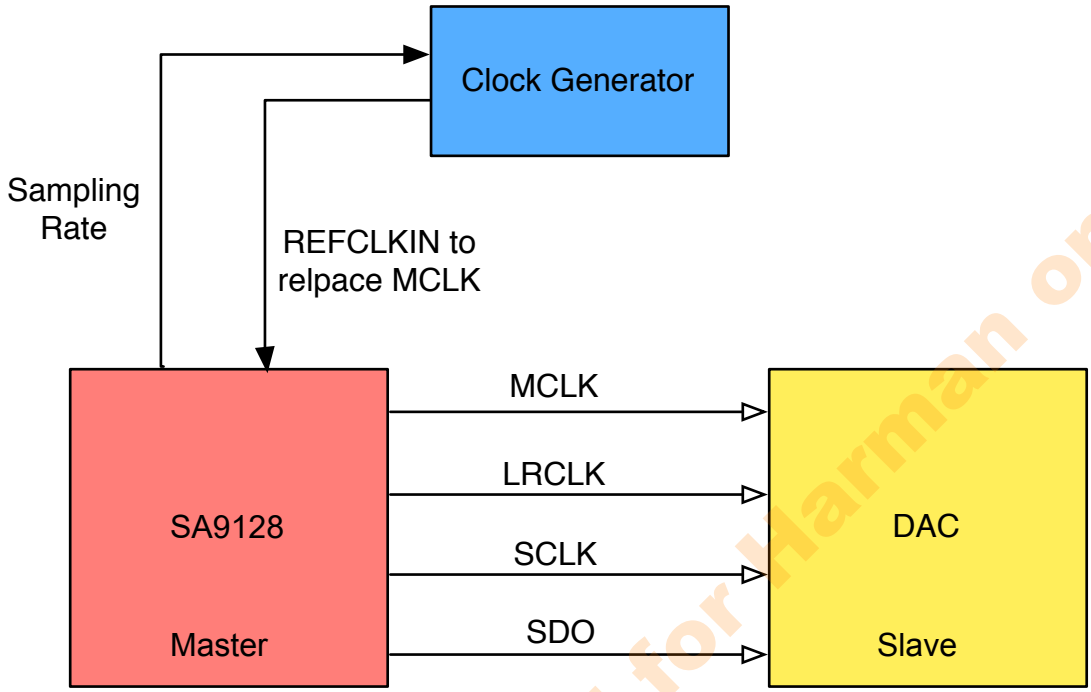
SA9128 I2S Master Mode connection

■ **Slave Mode**

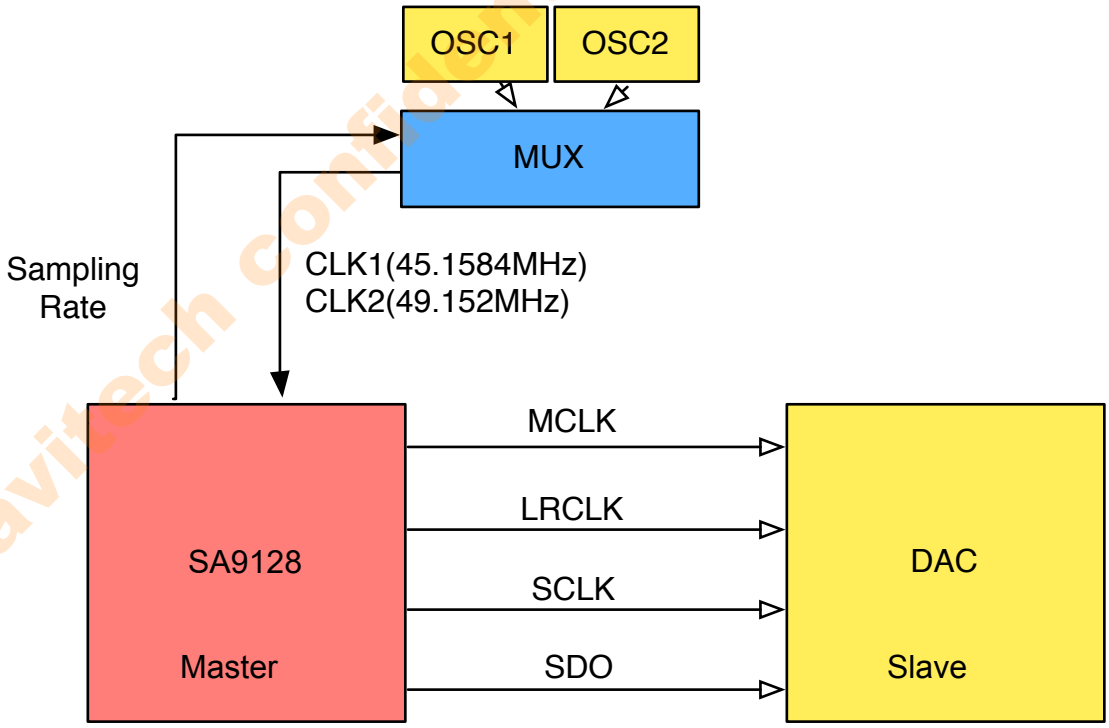


SA9128 I2S Slave Mode connection

Serial Audio Interfaces Configuration-DAC

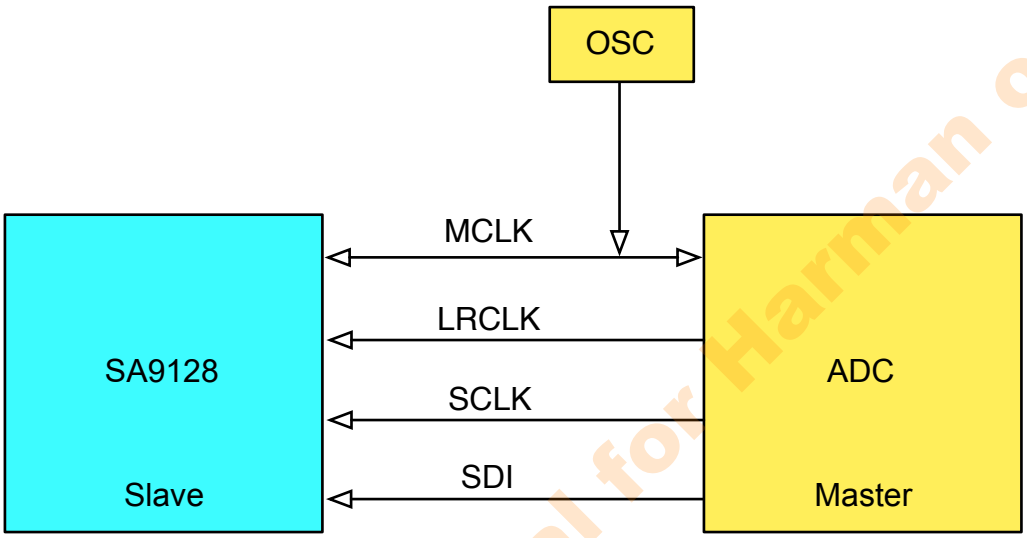


Master Mode (with external REFCLKIN), Mode 0



Master Mode (with external REFCLKIN), Mode 1

Serial Audio Interfaces Configuration-ADC



S/PDIF RX Interfaces

SA9128 support one S/PDIF RX interfaces, each can support up to 24-bit 48K sampling rate. Built in IEC60958 professional SPDIF RX,

- AES/EBU supported
- 32/ 44.1/ 48 KHz sampling rates
- 24 bit resolution

I²C Master Interfaces

One serial I²C master is supported in SA9128 to control external peripheral devices (EEPROM). SA9128 need an EEPROM to load Firmware code from it to SA9128.

General Purpose Interface IN /OUT

Seven GPIOs pins are supported that can be controlled by standard USB HID requests.

GPIOs	Description
GPIO1	Use for reset DAC
GPIO2	USB speed selector, "0" : High-speed, “1”: Full-speed
GPIO3	Selection of 49MHz, 45MHz external clocks for reference input pin ‘0’: 49Mhz, ‘1’:45MHz
GPIO0 / 4 / 7 / 8	General purpose interface I/O

Flag Signals

FLAGs	Definition
SOF_FLAG	User can check this pin to understand USB is in suspend or not 0: USB is in suspend 1: USB is in normal mode

Pin Assignment

Pin	Name	Pin	Name
1	VDD33_LDO	33	GPIO4
2	GND_LDO	34	GPIO7
3	VDD18_LDO	35	GPIO8
4	VDD33	36	RESETN
5	GND	37	VDD33
6	SPDIF_RX	38	SCL_M
7	VDD33	39	SDA_M
8	VDD18	40	DBCLK
9	SOF_FLAG	41	DDATA3
10	NC	42	DDATA2
11	NC	43	VDD18
12	REXT	44	VDD33
13	VDD33	45	DDATA1
14	VDD33	46	DDATA0
15	DP	47	DMCLK
16	DM	48	DLRCK
17	GND	49	ABCLK
18	XI	50	ADATA
19	XO	51	AMCLK
20	VDD18	52	VDD33
21	VDD33	53	ALRCK
22	GND	54	VDD33
23	GND	55	REFCLKIN
24	VDD33	56	VDD18
25	GND	57	SPICLK
26	VDD33	58	SPICS
27	GPIO0	59	SPIMOSI
28	VDD18	60	SPIMISO
29	VDD33	61	TEST0
30	GPIO1	62	TEST1
31	GPIO2 / USB (FS) SEL	63	TEST2
32	GPIO3	64	TEST3

Pin Description

Pin	Name	I/O/P	Description
1	VDD33_LDO	P	LDO 3.3V Input
2	GND_LDO	P	LDO Ground
3	VDD18_LDO	P	LDO 1.8V Output
4	VDD33	P	SPDIF RX power
5	GND	P	SPDIF RX ground
6	SPDIF_RX	I	S/PDIF RX input
7	VDD33	P	I/O power
8	VDD18	P	Core power
9	SOF_FLAG	O	USB SOF(Start Of Frame) indicator
10	NC	-	No connect
11	NC	-	No connect
12	REXT	I	Connect 270ohm resistor to ground
13	VDD33	P	USB2.0 PHY power
14	VDD33	P	USB2.0 PHY power
15	DP	I/O	USB2.0 signals
16	DM	I/O	USB2.0 signals
17	GND	P	USB2.0 PHY ground
18	XI	I	12MHz X'stal
19	XO	O	12MHz X'stal
20	VDD18	P	USB2.0 PHY power
21	VDD33	P	PLL power
22	GND	P	PLL ground
23	GND	P	PLL ground
24	VDD33	P	PLL power
25	GND	P	PLL ground
26	VDD33	P	PLL power
27	GPIO0	OD, I/O	General purpose I/O
28	VDD18	P	Core power
29	VDD33	P	I/O power
30	GPIO1	OD, I/O	General purpose I/O
31	GPIO2 / USB (HS/FS) SEL	OD, I/O	Pull-low for USB High-speed Pull-high for USB Full-speed
32	GPIO3	OD, I/O	General purpose I/O

Pin	Name	I/O/P	Description
33	GPIO4	OD, I/O	General purpose I/O
34	GPIO7	OD, I/O	General purpose I/O
35	GPIO8	OD, I/O	General purpose I/O
36	RESETN	I	Power-on reset signal (active low)
37	VDD33	P	I/O power
38	SCL_M	I/O	Master I2C clock
39	SDA_M	I/O	Master I2C clock
40	DBCLK	I/O	I2S output BCLK
41	DDATA3	O	I2S output DATA3
42	DDATA2	O	I2S output DATA2
43	VDD18	P	Core power
44	VDD33	P	I/O power
45	DDATA1	O	I2S output DATA1
46	DDATA0	O	I2S output DATA0
47	DMCLK	O	I2S output MCLK
48	DLRCK	I/O	I2S output LRCK
49	ABCLK	I/O	I2S input BCLK
50	ADATA	I	I2S input DATA
51	AMCLK	I/O	I2S input MCLK
52	VDD33	P	I/O power
53	ALRCK	I/O	I2S input LRCLK
54	VDD33	P	I/O power
55	REFCLKIN	I	Optional external reference clock input
56	VDD18	P	Core power
57	SPICLK	O	SPI Clock
58	SPICS	O	SPI Chip select
59	SPIMOSI	O	SPI Master output / Slave input
60	SPIMISO	I	SPI Master input / Salve output
61	TEST0	I	normal mode : tied VDD33
62	TEST1	I	normal mode : tied GND
63	TEST2	I	normal mode : tied GND
64	TEST3	I	normal mode : tied GND

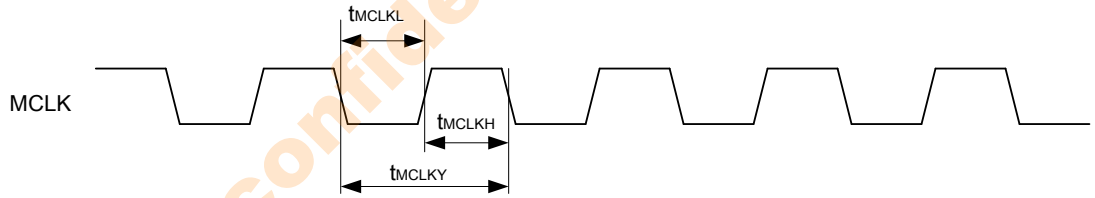
DC Characteristics

Test Conditions: Ta = 25°C; VDD33 = +3.0 ~ +3.6V; fs = 48 kHz-32bit sine wave

Parameter	Symbol	Test Condition	Min.	Max.	Unit
Input Low Voltage	VIL	VD33 = 3.3V		0.3*VDD33	V
Input High Voltage	VIH	VDD33 = 3.3V	0.7*VDD33		V
Output Low Voltage	VOL	IOL = 2mA		0.2	V
Output High Voltage	VOH	IOH = -2mA	VDD33-0.2		V
Input Low Leakage Current	IIL	VIN = 0V VDD33 = 3.6V	-10	10	uA
Input High Leakage Current	IIH	VIN = 3.6V VDD33 = 3.6V	-10	10	uA
Operation Power Current		VDD33 = 3.3V VDD18 = Int. LDO		TBD	mA
Operation Power Current		VDD33 = 3.3V VDD18 = Ext. DC-DC		TBD	mA

AC Timing Characteristics

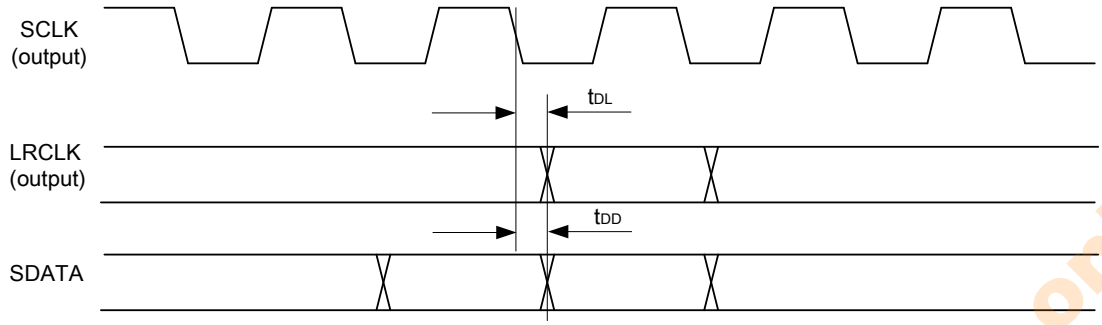
1. System Clock Timing



Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24-bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
MCLK System clock pulse width high	tMCLKL		41.13		ns
MCLK System clock pulse width low	tMCLKH		40.23		ns
MCLK System clock cycle time	tMCLKY		81.36		ns

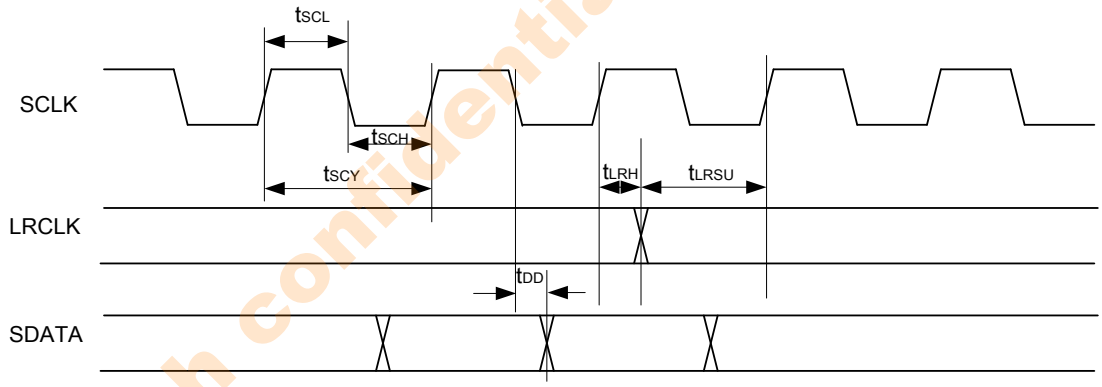
2. Audio Interface Timing – Master Mode



Test Conditions: VDD = V, VSS = 0V, TA = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24-bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
LRCLK propagation delay from SCLK falling edge	tDL	5			ns
SDATA propagation delay from SCLK falling edge	tDDA	5			ns

3. Audio Interface Timing – Slave Mode



Test Conditions: VDD = V, VSS = 0V, TA = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24-bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
SCLK cycle time	tSCY	293	325	358	ns
LRCLK pulse width high	tSCH	144	163	179	ns
SCLK pulse width low	tSCL	144	163	179	ns

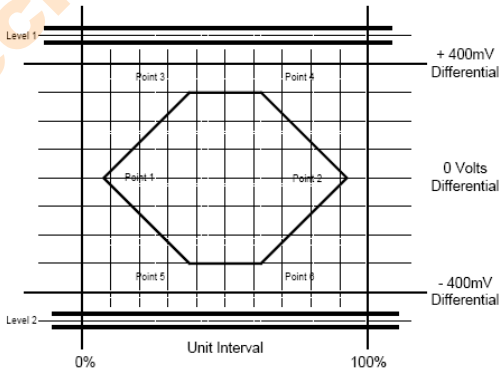
LRCLK set-up time to SCLK rising edge	tLRSU	10			ns
LRCLK hold time from SCLK rising edge	tLRH	10			ns
SDATA propagation delay from SCLK falling edge	tDD	5			ns

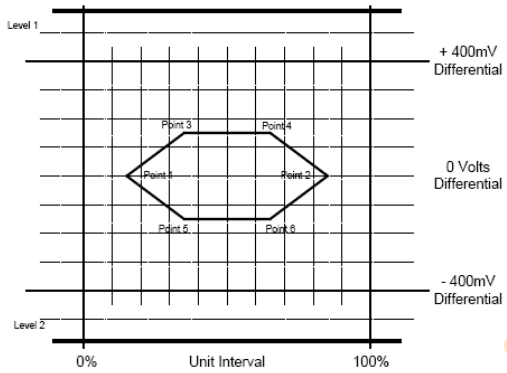
Dynamic Electrical Characteristics: (DP/DM)

Driver Characteristics:

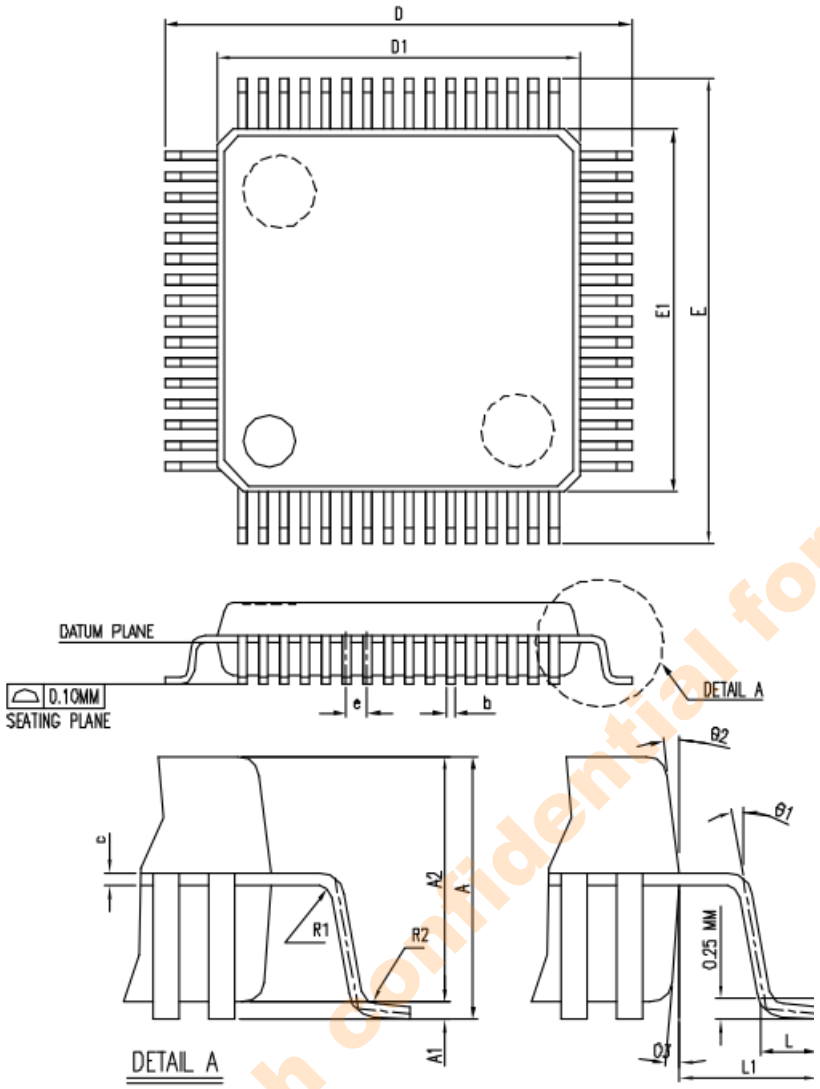
Symbol	Parameter	Min	Max	Unit
High-speed Mode				
t_{HSR}	High-speed differential rise time (10% - 90%)	500	-	ps
t_{HSF}	High-speed differential fall time (10% - 90%)	500	-	ps
Full-speed Mode				
t_{FR}	Rise Time for DP/DM	4	20	ns
t_{FF}	Fall Time for DP/DM	4	20	ns
t_{FRFM}	Differential rise/fall Time Matching (t_{FR} / t_{FF})	90	110	%
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V

Driver Timing/Receiver timing:

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver timing						
High-speed mode						
Driver waveform requirement	See the eye pattern of template 1 (described in the USB 2.0 spec.) 	Follow template 1 described in USB specification Rev 2.0. <table><tr><th></th><th>Voltage Level (D+ - D-)</th><th>Time (% of Unit Interval)</th></tr><tr><td>Level 1</td><td>525 mV in UI following a transition, 475 mV in all others</td><td>N/A</td></tr><tr><td>Level 2</td><td>-525 mV in UI following a transition, -475 in all others</td><td>N/A</td></tr><tr><td>Point 1</td><td>0 V</td><td>7.5% UI</td></tr><tr><td>Point 2</td><td>0 V</td><td>92.5% UI</td></tr><tr><td>Point 3</td><td>300 mV</td><td>37.5% UI</td></tr><tr><td>Point 4</td><td>300 mV</td><td>62.5% UI</td></tr><tr><td>Point 5</td><td>-300 mV</td><td>37.5% UI</td></tr><tr><td>Point 6</td><td>-300 mV</td><td>62.5% UI</td></tr></table>			
Full-speed mode						

<table>
<tr><td>Propagation delay (VI, FSE 0, OE to DP, DM)</td><td>For the detailed description of VI, FSE 0, and OE, (please refer to the USB 1.1 spec.)</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
<tr><td colspan="6">Receiver timing</td></tr>
<tr><td colspan="6">High-speed mode (template 4, USB 2.0 spec.)</td></tr>
<tr><td>Data source jitter and receiver jitter tolerance</td><td colspan="2">See the eye pattern of template 4 (described in the USB 2.0 spec.)
 
</td><td colspan="3">Follow template 4 described in USB specification Rev 2.0.
<table><tr><th></th><th>Voltage Level (D+ - D-)</th><th>Time (% of Unit Interval)</th></tr><tr><td>Level 1</td><td>575 mV</td><td>N/A</td></tr><tr><td>Level 2</td><td>-575 mV</td><td>N/A</td></tr><tr><td>Point 1</td><td>0 V</td><td>15% UI</td></tr><tr><td>Point 2</td><td>0 V</td><td>85% UI</td></tr><tr><td>Point 3</td><td>150 mV</td><td>35% UI</td></tr><tr><td>Point 4</td><td>150 mV</td><td>65% UI</td></tr><tr><td>Point 5</td><td>-150 mV</td><td>35% UI</td></tr><tr><td>Point 6</td><td>-150 mV</td><td>65% UI</td></tr></table></td></tr>
<tr><td colspan="6">Full-speed mode</td></tr>
<tr><td>$t_{PLH(rcv)}$
$t_{PHL(rcv)}$</td><td>Receiver propagation delay (DP; DM to RX_RCV)</td><td>For the detailed description of RCV, (please refer to the USB 1.1 spec.)</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
<tr><td>$t_{PLH(single)}$
$t_{PHL(single)}$</td><td>Receiver propagation delay (DP; DM to VOP, VON)</td><td>-</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
</table>

TQFP 64 MECHANICAL DATA



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.0019		0.0059
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09		0.20	0.0035		0.0078
e	0.40 BASIC			0.016 BASIC		
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.0031		
R2	0.08		0.20	0.0031		0.0078
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
JEDEC	MS-026 (BBD)					

*NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

SA9128