# SA9123L USB Audio Streaming Controller

## 1. Features

- Supply Range of 1.8 V to 3.3 V
- Control and I/O
  - I2C bus
  - FWIOs
- Support iAP2
- USB 2.0 High-Speed Compliant
- USB Audio Class v1.0 and v2.0 supported
- Support Dynamic Consumption Adjustment
- One interrupt endpoint for HID
- Support resolutions up to 24-bit and sampling rates up to 192KHz
- Two I2S input and two I2S output pairs for PCM
  - Independent sample rates for each pair
  - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192 KHz sampling rates
  - 16/24 bit resolution
- 64-pin LQFP package

## 2. Description

- Mobile Phone Audio Accessary
- Type-C Audio
- USB Audio
- iDevice

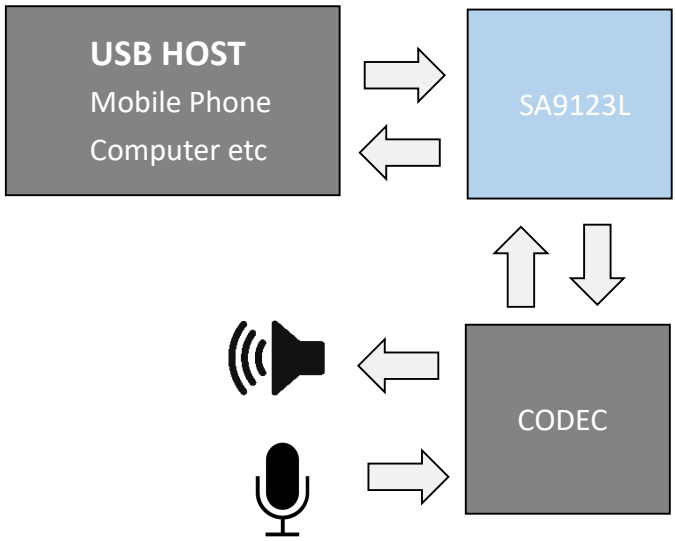
## 3. Applications

The SA9123L is a high performance up to 24bit, 192KHz PCM streaming USB High-Speed compliant audio steaming controller. It features one IEC60958 S/PDIF transmit streaming output. The SA9123L is ideal for both one stereo-in and one stereo-out professional digital audio interface applications.

**Device Information**

| PART NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| SA9123L-64LQ | LQFP | 7mm x 7mm |

## 4. Simplified Schematic



## Table of Contents

## 5. Pin Configuration and Functions

### 5.1 Pin Functions

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | TQFP-64 | | |
| | | | |
| VDD33 | 1 | Power | Power on Reset |
| GND | 2 | Power | I/O ground |
| VDD18 | 3 | Power | Core power |
| VDDIO | 4 | Power | I/O power |
| GND | 5 | Power | I/O ground |
| NC | 6 | - | Floating |
| VDDIO | 7 | Power | I/O power |
| VDD18 | 8 | Power | Core power |
| SOF_FLAG | 9 | O | USB SOF(Start Of Frame) indicator |
| NC | 10 | - | NC |
| NC | 11 | - | NC |
| REXT | 12 | I | Connect 270ohm resistor to ground |
| VDD33 | 13 | Power | USB2.0 PHY power |
| VDD33 | 14 | Power | USB2.0 PHY power |
| DP | 15 | I/O | USB2.0 signals |
| DM | 16 | I/O | USB2.0 signals |
| GND | 17 | Power | USB2.0 PHY ground |
| XI | 18 | I/O | 12MHz X'stal |
| XO | 19 | I/O | 12MHz X'stal |
| VDD18 | 20 | Power | USB2.0 PHY core power |
| VDD33 | 21 | Power | PLL power |
| GND | 22 | Power | PLL ground |
| GND | 23 | Power | PLL ground |
| VDD33 | 24 | Power | PLL power |
| GND | 25 | Power | PLL ground |
| VDD33 | 26 | Power | PLL power |
| GPIO0 | 27 | I/O | Firmware assign function I/O port*1 |

| | | | |
|---|---|---|---|
| VDD18 | 28 | Power | Core power |
| VDDIO | 29 | Power | I/O power |
| GPIO1 | 30 | I/O | Firmware assign function I/O port*1 |
| GPIO2 | 31 | I/O | Firmware assign function I/O port*1 |
| GPIO3 | 32 | I/O | Firmware assign function I/O port*1 |
| GPIO4 | 33 | I/O | Firmware assign function I/O port*1 |
| GPIO5 | 34 | I/O | Firmware assign function I/O port*1 |
| GPIO6 | 35 | I/O | Firmware assign function I/O port*1 |
| GPIO7 | 36 | I/O | Firmware assign function I/O port*1 |
| GPIO8 | 37 | I/O | For Apple CP reset |
| RESETN | 38 | I | Power-on reset signal (active low) |
| VDDIO | 39 | Power | I/O power |
| SCL_M | 40 | I/O | Master I2C clock |
| SDA_M | 41 | I/O | Master I2C data |
| DBCLK | 42 | I/O | I2S output BCLK |
| VDD18 | 43 | Power | Core power |
| NC | 44 | - | Floating |
| DDATA | 45 | O | I2S output DATA |
| DMCLK | 46 | I/O | I2S output MCLK |
| DLRCK | 47 | I/O | I2S output LRCLK |
| SPDIFTX | 48 | O | SPDIFOUT |
| ABCLK | 49 | I/O | I2S input BCLK |
| ADATA | 50 | I | I2S input DATA pin |
| AMCLK | 51 | I/O | I2S input MCLK |
| NC | 52 | - | Floating |
| ALRCK | 53 | I/O | I2S input LRCLK |
| SCL_S | 54 | I/O | Slave I2C CLK |
| SDA_S | 55 | I/O | Slave I2C SDA |
| VDDIO | 56 | Power | I/O power |
| REFCLKIN | 57 | I | Optional external reference clock input |
| VDD18 | 58 | Power | Core power |
| TEST1 | 59 | I | Normal Operation need pull-high |
| TEST2 | 60 | I | Normal Operation need pull-down |
| TEST3 | 61 | I | Normal Operation need pull-down |
| TEST4 | 62 | I | Normal Operation need pull-down |
| TEST5 | 63 | I | Normal Operation need pull-down |

| | | | |
|---|---|---|---|
| TEST6 | 64 | I | Normal Operation need pull-down |

*1. All FWIOs are firmware assign function input/output, contact FAE to customize.

# 6. Specifications

## 6.1 DC Characteristics

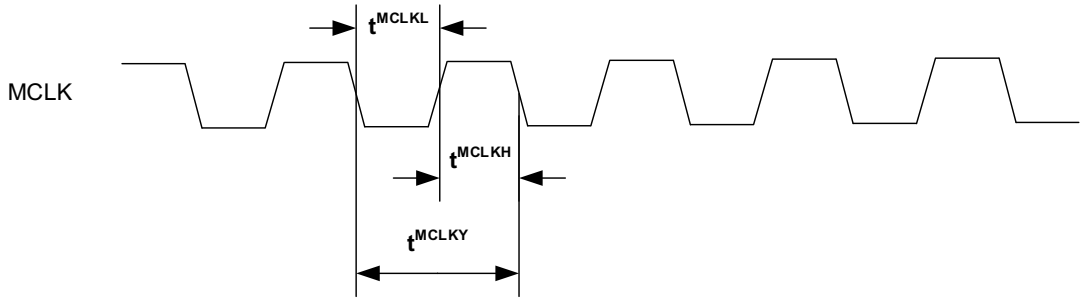
Test Conditions: Ta = 25°C; VDD33 = +3.0 ~ +3.6V; fs = 48 kHz-32bit sine wave

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input Low Voltage | VIL | VDD33 = 3.3V | | 0.3*VDD33 | V |
| Input High Voltage | VIH | VDD33 = 3.3V | 0.7*VDD33 | | V |
| Output Low Voltage | VOL | IOL = 2mA | | 0.2 | V |
| Output High Voltage | VOH | IOH =---2mA | VDD33---0.2 | | V |
| Input Low Leakage Current | IIL | VIN = 0V<br>VDD33 = 3.6V | ---10 | 10 | uA |
| Input High Leakage Current | IIH | VIN = 3.6V<br>VDD33 = 3.6V | ---10 | 10 | uA |
| Operation Current | Idle*1 | VDD33 = 3.3V<br>VDD18 = Ext. DC-DC | | 25 | mA |
| Operation Current | Up to 192KHz Playback*1 | VDD33 = 3.3V<br>VDD18 = Ext. DC-DC | | 45 | mA |
| Suspend Current | Suspend | Total 3.3V rail | 2 | 3 | mA |
| | | Total 1.8V rail | 2 | 3 | |

*1 The power mode is controlled by F/W.

## 6.2 AC Timing Characteristics

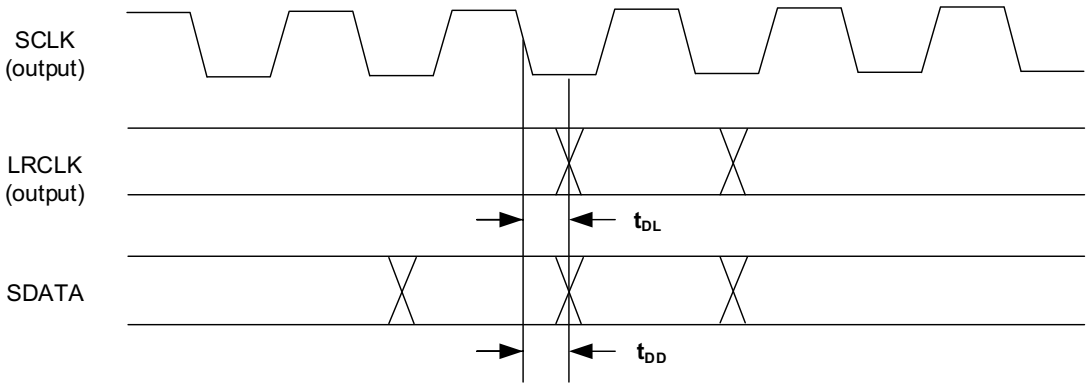
### 6.2.1 System Clocking Timing




Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24--bit data.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| MCLK System clock pulse width high | $t^{MCLKL}$ | | 41.13 | | ns |
| MCLK System clock pulse width low | $t^{MCLKH}$ | | 40.23 | | ns |
| MCLK System clock cycle time | $t^{MCLKY}$ | | 81.36 | | ns |

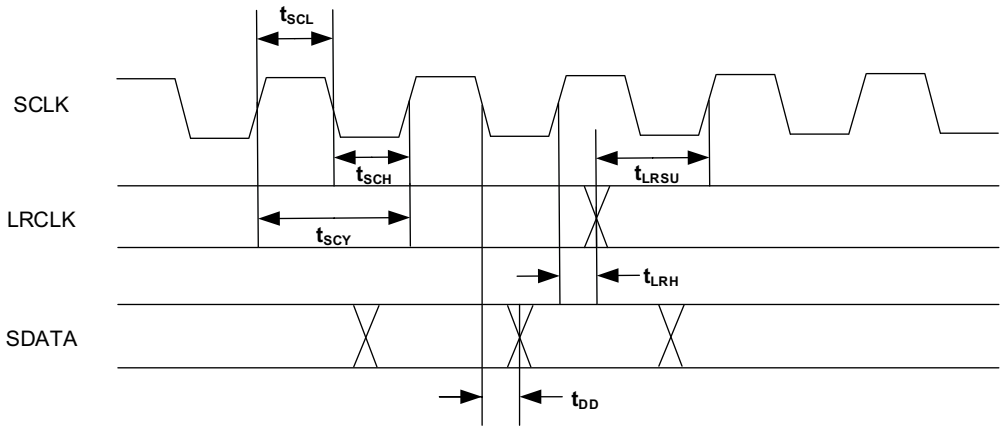
### 6.2.2 Audio Interface Timing – Master Mode




Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24--bit data.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| LRCLK propagation delay from SCLK falling edge | $t_{DL}$ | 5 | | | ns |
| SDATA propagation delay from SCLK falling edge | $t_{DD}$ | 5 | | | ns |

### 6.2.3 Audio Interface Timing – Slave Mode




Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24--bit data.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| SCLK cycle time | $t_{SCY}$ | 293 | 325 | 358 | ns |
| LRCLK pulse width high | $t_{SCH}$ | 144 | 163 | 178 | ns |
| SCLK pulse width low | $t_{SCL}$ | 144 | 163 | 179 | ns |
| LRCLK set-up time to SCLK rising edge | $t_{LRSU}$ | 10 | | | |
| LRCLK hold time from SCLK rising edge | $t_{LRH}$ | 10 | | | |
| SDATA propagation delay from SCLK falling edge | $t_{DD}$ | 5 | | | |

## 6.3 Dynamic Electrical Characteristics (DP/DM)

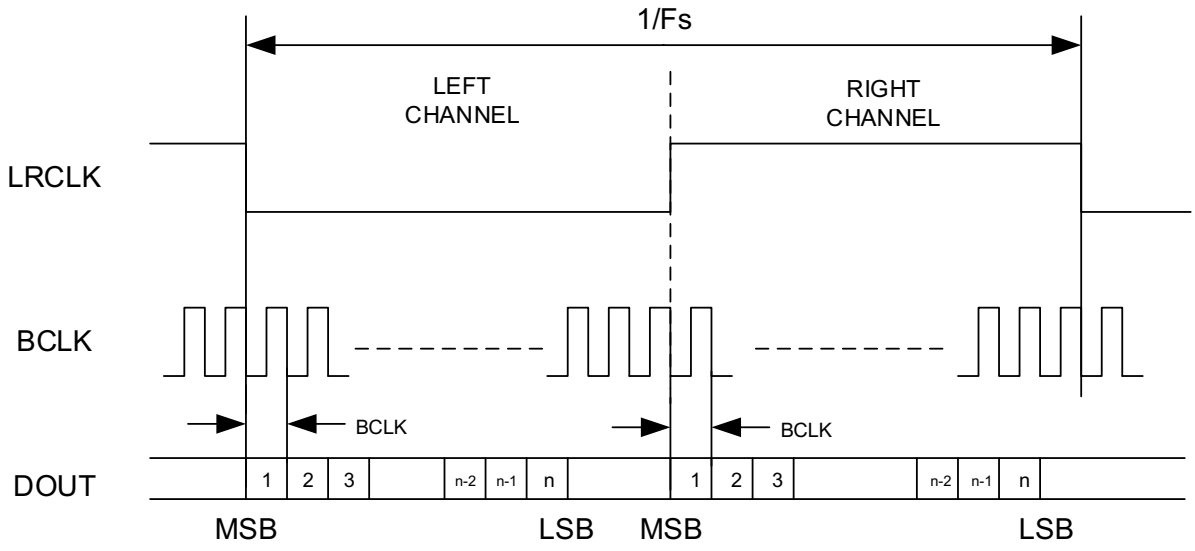
Driver Characteristics:

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| **High – Speed Mode** | | | | |
| High – speed differential rise time (10% - 90%) | $t_{HSR}$ | 500 | | ps |
| High – speed differential fall time (10% - 90%) | $t_{HSF}$ | 500 | | ps |
| **Full – Speed Mode** | | | | |
| Rise Time for DP/DM | $t_{FR}$ | 4 | 20 | ns |
| Fall Time for DP/DM | $t_{FF}$ | 4 | 20 | ns |
| Differential Rise/Fall Time Matching ($t_{FR}/t_{FF}$) | $t_{FRFM}$ | 90 | 110 | % |
| Output Signal Crossover Voltage | $V_{CRS}$ | 1.3 | 2.0 | V |

# 7. Serial Audio Interfaces Formats

## 7.1 I2S Format

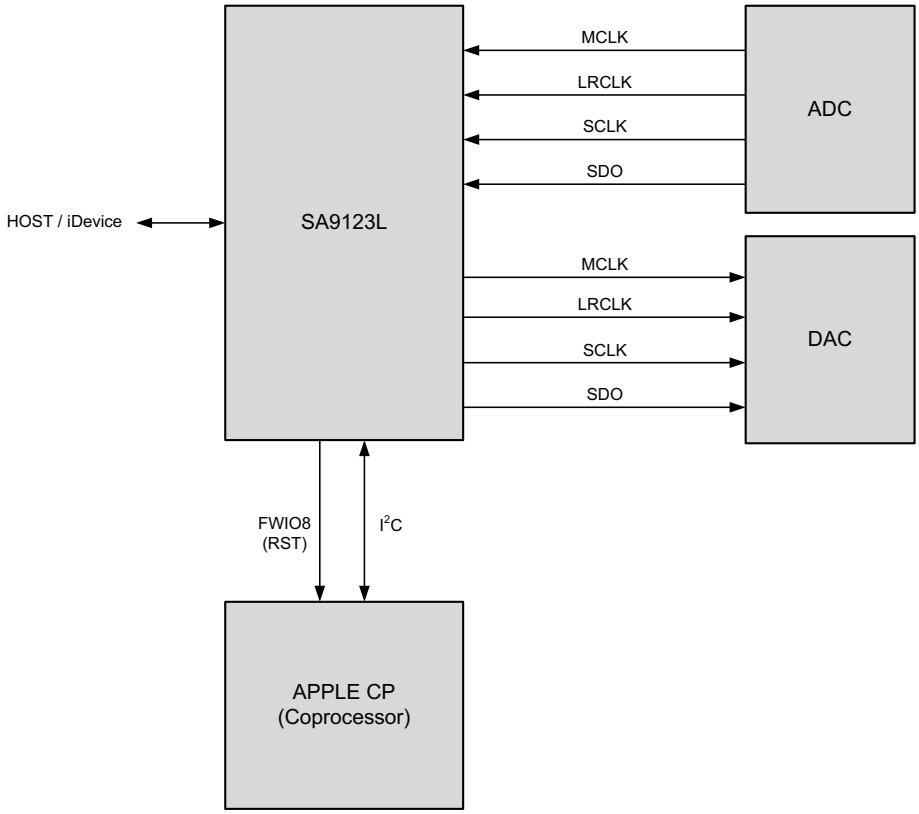
In I2S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.



## 8. iDevice Support

Apple strongly recommends the use of digital audio paths to and from accessories. Apple device in USB Host Mode audio is the recommended approach. SA9123L will authenticate and identify itself to Apple device using iAP1/iAP2 CP before the iDevice will enumerate and start using USB Audio interface.

- Support 16 /24-bit linear PCM
- Support 44.1 / 48KHz sampling rate and up to 192KHz for future.
- Support input and output audio interface
- Support Volume Control Feature Unit
- Support iAP1 and iAP2 by CP2.0B and CP2.0C.



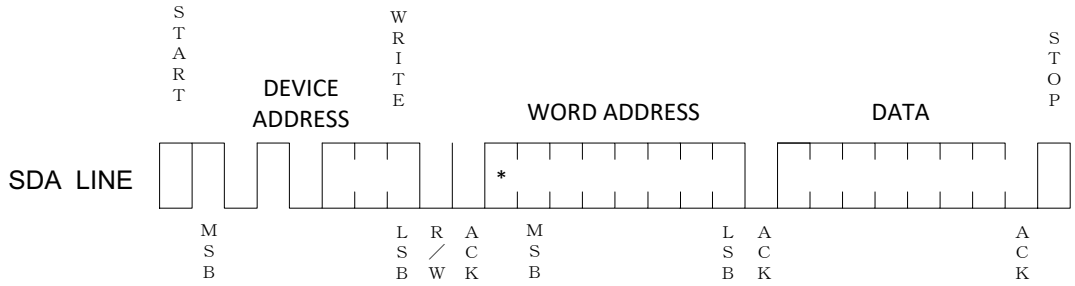

**Digital USB Audio Application For iDevice**

## 9. I²C Master Interfaces

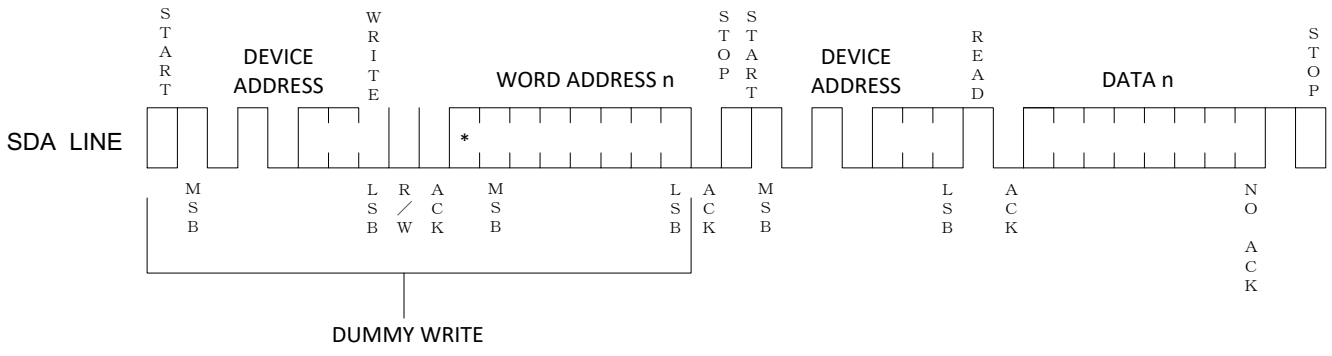
One serial I²C master is supported in SA9123L to control external peripheral devices (EEPROM). SA9123L need an EEPROM to load Firmware code from it.

SA9123L support use I²C Master Interfaces to read/write CP to support Apple MFi.

**Byte Write**




**Random Read**



## 10. Chip Status Flags

SA9123L provide these pins for display chip status flag

| FLAGs | Definition |
|---|---|
| SOF_FLAG | User can check this pin to understand USB is in suspend or not<br>0: USB is in suspend<br>1: USB is in normal mode |

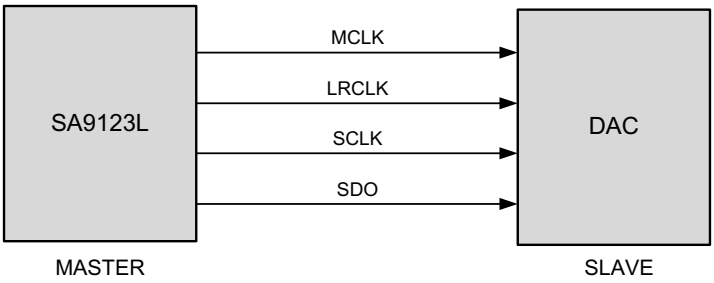
# 11. Application and Implementation

## 11.1 Typical Application

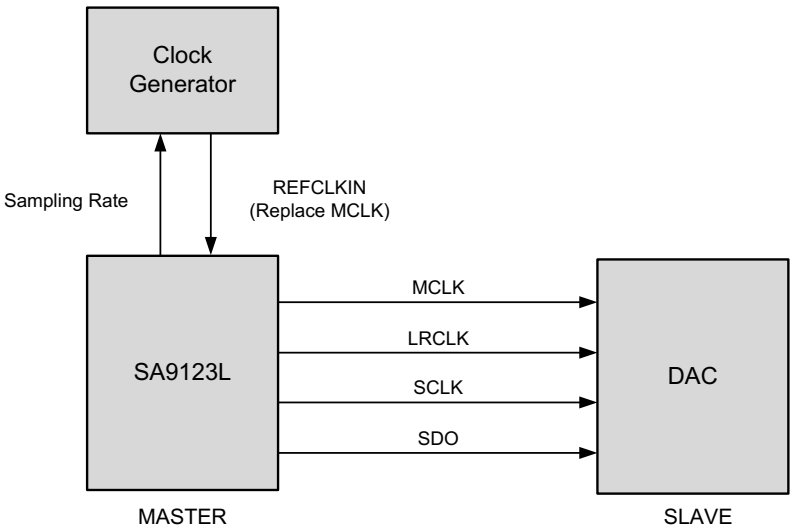
Typical application for SA9123L connecting with DAC / ADC. The following section shows how the SA9123L works with different serial data format including PCM

### 11.1.1 Serial Audio Interfaces Configuration-DAC (Master Mode)

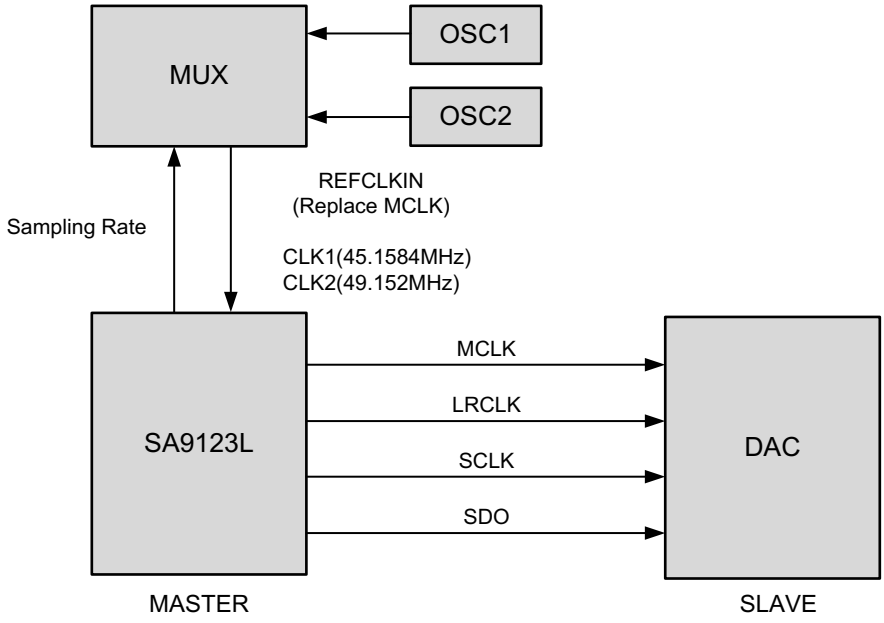
SA9123L supports master mode for following configuration




**SA9123L I²S Mater Mode Connection**



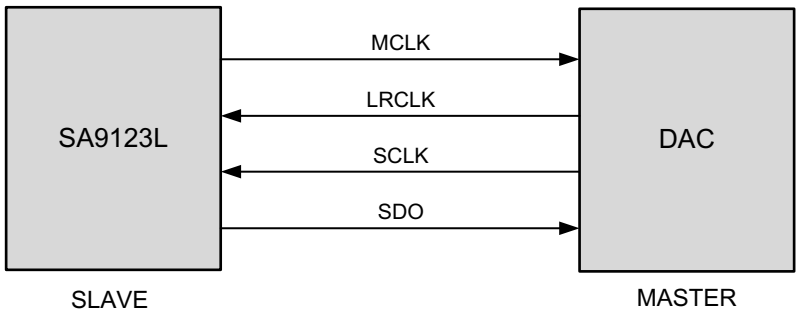

**Master Mode (with external REFCLKIN), Mode 0**




**Master Mode (with external REFCLKIN), Mode 1**

### 11.1.2 Serial Audio Interfaces Configuration-DAC (Slave Mode)

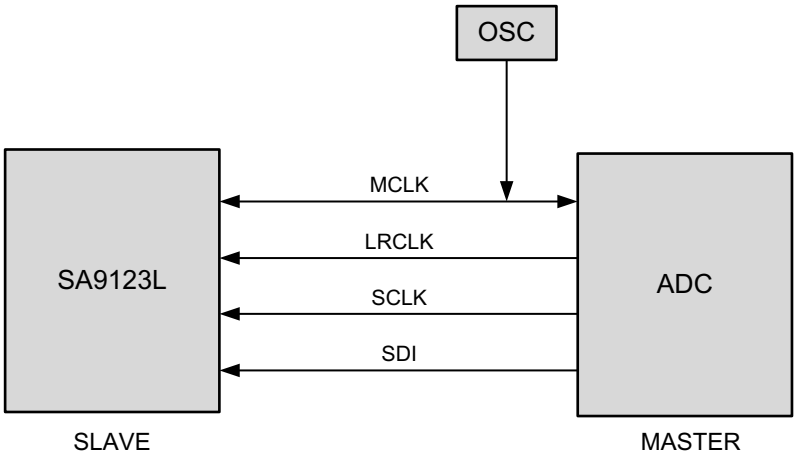
SA9123L supports slave mode for following configuration




**SA9123L I²S Slave Mode Connection**

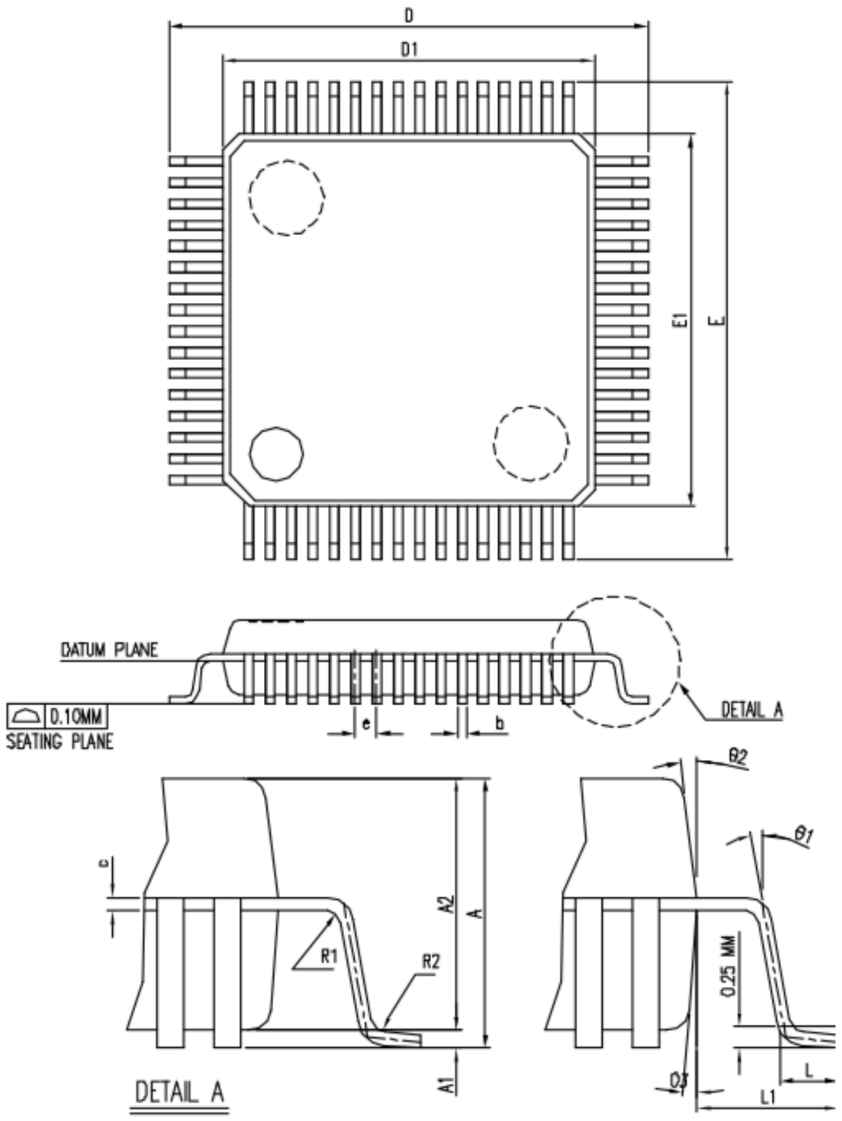
### 11.1.3 Serial Audio Interfaces Configuration-ADC

SA9123L supports slave mode for following configuration




**SA9123L I²S Slave Mode Connection**

## 12. Package Outline (LQFP)




| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.0019 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0078 |
| e | 0.40 BASIC | | | 0.016 BASIC | | |
| D | 9.00 BASIC | | | 0.354 BASIC | | |
| D1 | 7.00 BASIC | | | 0.276 BASIC | | |
| E | 9.00 BASIC | | | 0.354 BASIC | | |
| E1 | 7.00 BASIC | | | 0.276 BASIC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF. | | | 0.039 REF. | | |
| R1 | 0.08 | | | 0.0031 | | |
| R2 | 0.08 | | 0.20 | 0.0031 | | 0.0078 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | | | 0° | | |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| JEDEC | MS-026 (BBD) | | | | | |

*NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.