ES7241D

High Performance Stereo Audio ADC

FEATURES

- High performance multi-bit delta-sigma audio ADC
- 100 dB signal to noise ratio
- -85 dB THD+N
- 3 Vpp analog input
- 24-bit, 8 to 200 kHz sampling frequency
- I^2S/LJ master or slave serial data port
- 256/384Fs and other non standard audio system clocks
- Low power standby mode

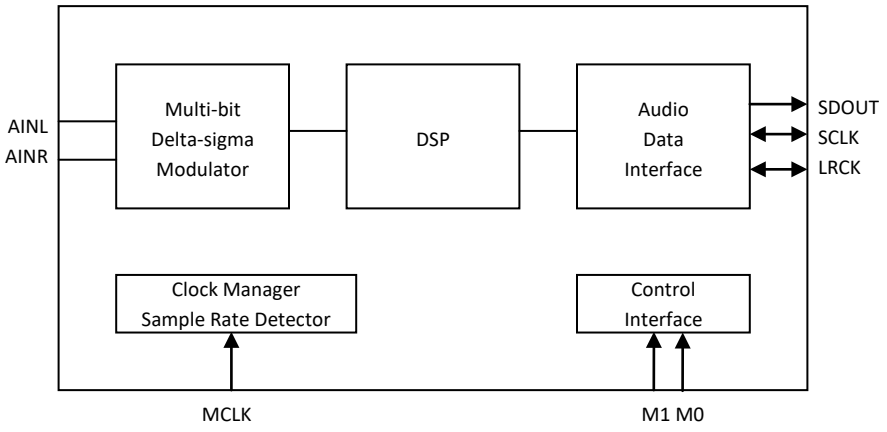
APPLICATIONS

- Soundbar
- Audio Interface
- Digital TV
- A/V Receiver
- DVR
- NVR

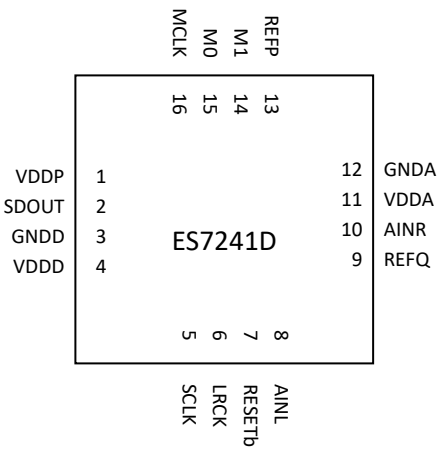
ORDERING INFORMATION

ES7241D -40°C ~ +85°C
QFN-16

BLOCK DIAGRAM

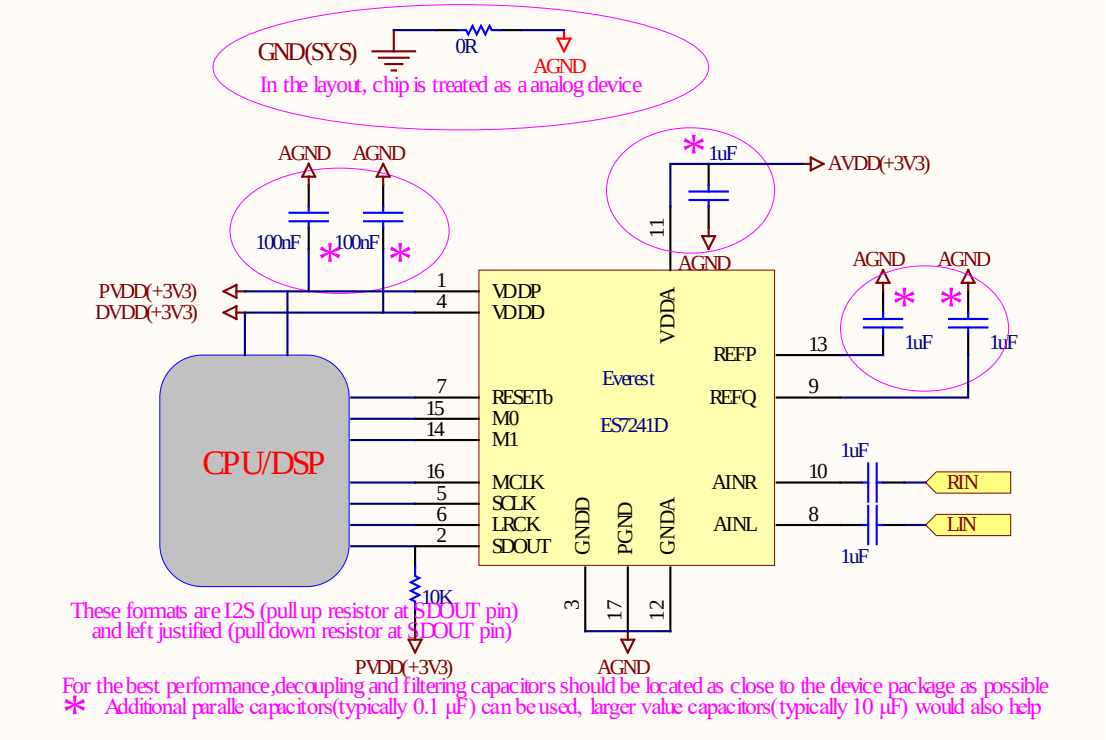


1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
M0, M1	15,14	I	Mode selection
MCLK	16	I	Master clock
SCLK	5	I/O	Serial data bit clock
LRCK	6	I/O	Serial data left and right channel frame clock
SDOUT	2	O	Serial data output
RESETb	7	I	Active low chip reset (low power)
AINL, AINR	8,10	I	Analog left and right inputs
VDDP	1	I	Power supply for the digital input and output
VDDD/GNDD	4,3	I	Digital power supply
VDDA/GNDA	11,12	I	Analog power supply
REFP	13	O	Filtering capacitor connection
REFQ	9	O	Filtering capacitor connection

2. TYPICAL APPLICATION CIRCUIT



3. CLOCK MODES AND SAMPLING FREQUENCIES

The device can work either in master clock mode or slave clock mode by setting mode control pins M1 and M0 according to Table 1.

Table 1 Mode Control

Pin	Pin Description
M1:M0	00 – master clock mode, single speed mode 01 – master clock mode, double speed mode 10 – master clock mode, quad speed mode 11 – slave clock mode, all speed modes

In master mode, LRCK and SCLK are derived internally from MCLK. The available MCLK/LRCK ratios are listed in Table 2. SCLK/LRCK ratio is always 64 in master mode.

Table 2 Master Mode Sampling Frequencies and MCLK/LRCK Ratio

Speed Mode	Sampling Frequency	MCLK/LRCK Ratio
Single Speed	8kHz – 50kHz	256
Double Speed	50kHz – 100kHz	128
Quad Speed	100kHz – 200kHz	64

In slave mode, LRCK and SCLK are supplied externally. LRCK and SCLK must be synchronously derived from the system clock with some specific rates. The device can auto detect MCLK/LRCK ratio according to Table 3. The device only supports the MCLK/LRCK ratios listed in Table 3. The SCLK/LRCK ratio is normally 64.

Table 3 Slave Mode Sampling Frequencies and MCLK/LRCK Ratio

Speed Mode	Sampling Frequency	MCLK/LRCK Ratio
Single Speed	8kHz – 50kHz	256, 384, 512, 768, 1024
Double Speed	50kHz – 100kHz	128, 192
Quad Speed	100kHz – 200kHz	64

4. POWER UP AND POWER DOWN

RESETb pin active low will put the device in power down mode. During power-up, RESETb pin should be hold at low level to keep the device in reset until the power supplies, clocks and mode selection pins are stable.

5. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the output from the ADC through LRCK, SCLK and SDOUT pins. These formats are I^2S (pull up resistor at SDOUT pin) and left justified (pull down resistor at SDOUT pin). ADC data is out at SDOUT on the falling edge of

SCLK. The relationships of SDOUT (SDATA), SCLK and LRCK with these formats are shown through Figure 1 to Figure 2.

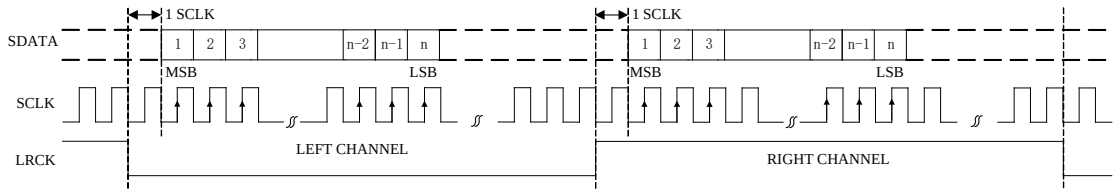


Figure 1 I^{2}S Serial Audio Data Format Up To 24-bit

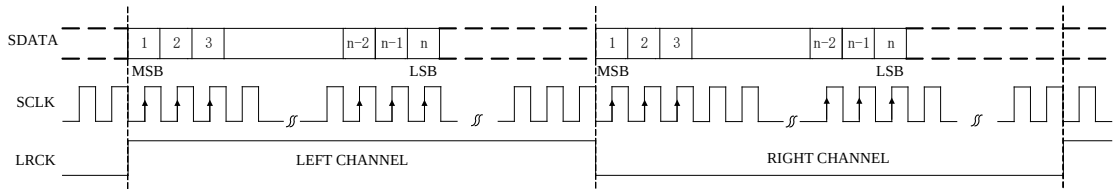


Figure 2 Left Justified Serial Audio Data Format Up To 24-bit

6. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	GNDA-0.3V	VDDA+0.3V
Digital Input Voltage Range	GNDD-0.3V	VDDP+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDDA	3.0	3.3	3.6	V
VDDD	3.0	3.3	3.6	V
VDDP	1.6	1.8/3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDDA=3.3V, VDDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	95	100	104	dB
THD+N	-88	-85	-75	dB
Channel Separation (1KHz)	95	100	105	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Quad Speed				
Passband	0		0.2083	Fs
Stopband	0.8958			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input Level		1.084		Vrms
Input Impedance		20		KΩ

POWER CONSUMPTION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDDD=3.3V, VDDP=3.3V, VDDA=3.3V		22		mA
Power Down Mode				
VDDD=3.3V, VDDP=3.3V, VDDA=3.3V		28		uA

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle (Note 1)		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SCLK falling to SDOUT valid VDDD=3.3V	T_{SDO}		16	ns
LRCK edge to SDOUT valid (Note 2) VDDD=3.3V	T_{LDO}		11	ns

Note 1: one SCLK period of high time in DSP/PCM modes.

Note 2: only apply to MSB of Left Justified or DSP/PCM mode B.

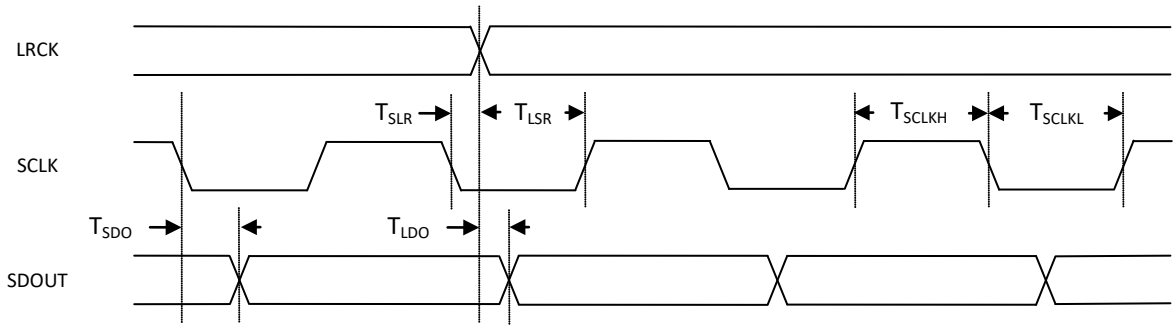
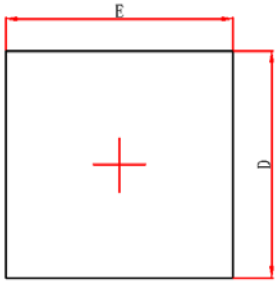


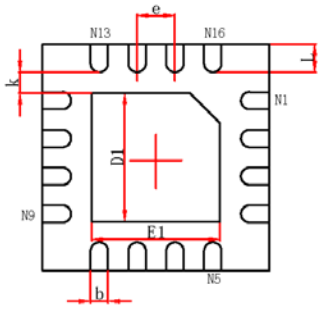
Figure 3 Serial Audio Port Timing

7. PACKAGE

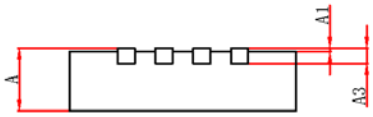
QFNWB3×3-16L(P0.50T0.75) PACKAGE OUTLINE DIMENSIONS



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.500TYP.	
L	0.300	0.500	0.012	0.020

8. CORPORATE INFORMATION

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