

High Performance PDM Stereo Audio ADC

FEATURES

- High performance advanced delta-sigma audio ADC
- Dynamic range: 95 dB @ 0 dB PGA, 91 dB @ 23 dB PGA, 86 dB @ 32 dB PGA
- -88 dB THD+N
- Low noise PGA
- 8 to 96 kHz sampling frequency
- Low power

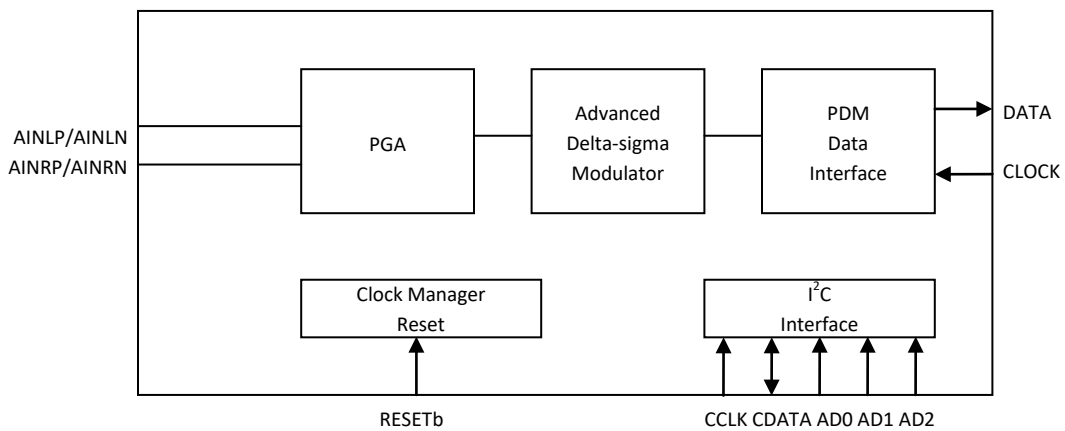
APPLICATIONS

- Mic Array
- Soundbar
- Audio Interface
- Digital TV
- A/V Receiver
- DVR
- NVR

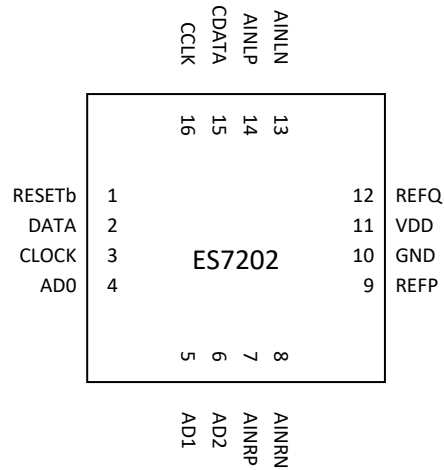
ORDERING INFORMATION

ES7202 -40°C ~ +85°C
QFN-16

BLOCK DIAGRAM



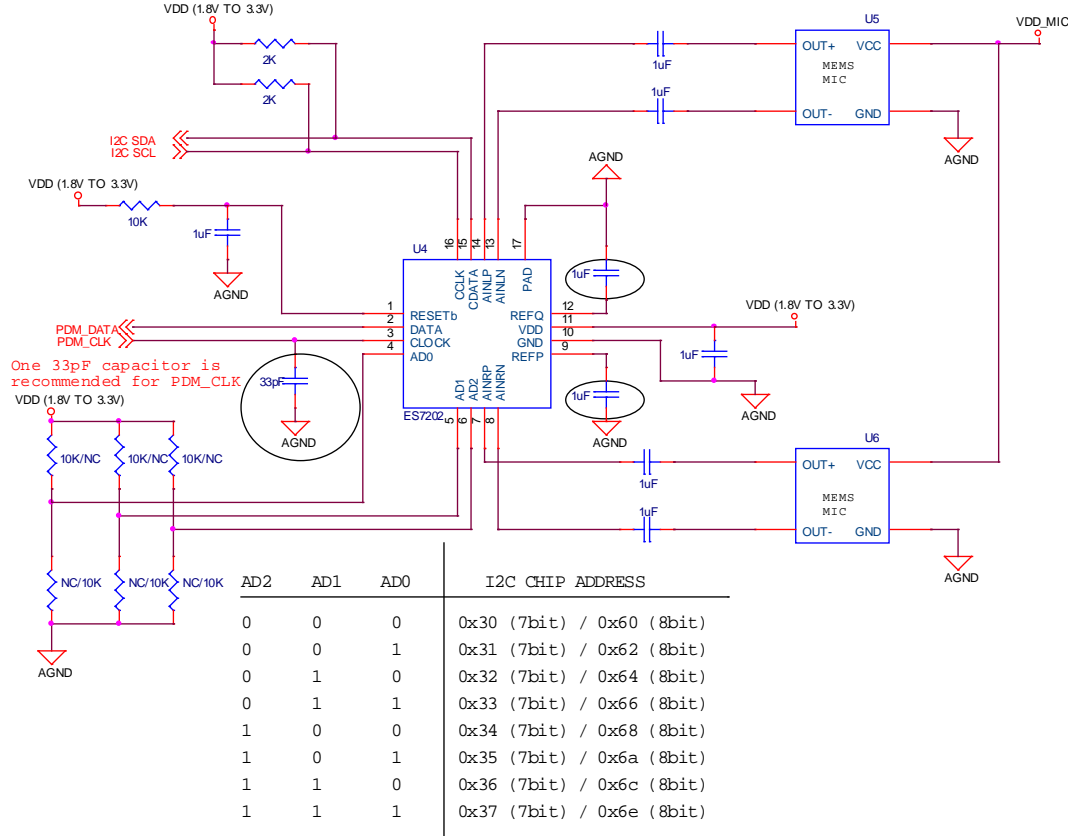
1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA	16, 15	I, I/O	I ² C clock and data
AD0, AD1, AD2	4, 5, 6	I	I ² C addresses
CLOCK, DATA	3, 2	I, O	PDM clock and data
RESETb	1	I	Active low reset
AINLP, AINLN	14, 13	I	Analog left inputs
AINRP, AINRN	7, 8	I	Analog right inputs
VDD, GND	11, 10	I	Power supply
REFP	9	O	Filtering capacitor connection
REFQ	12	O	Filtering capacitor connection

2. TYPICAL APPLICATION CIRCUIT

The filter capacitors on REFP and REFQ pins must be located as close to ES7202 package as possible. 4.7uF or 10uF capacitor is for better audio performance.



3. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I²C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I²C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 0110 x, where x equals AD2 AD1 AD0. The RW bit indicates the slave data transfer direction. Once an

acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I²C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I²C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0110 AD2 AD1 AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

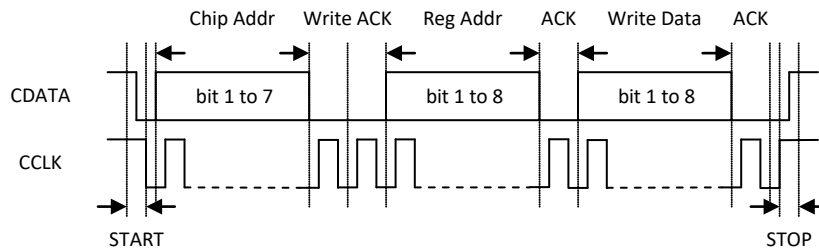


Figure 1a I²C Write Timing

Table 2 Read Data from Register in I²C Interface Mode

	Chip Address	R/W		Register Address		
Start	0110 AD2 AD1 AD0	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0110 AD2 AD1 AD0	1	ACK	Data	NACK	Stop

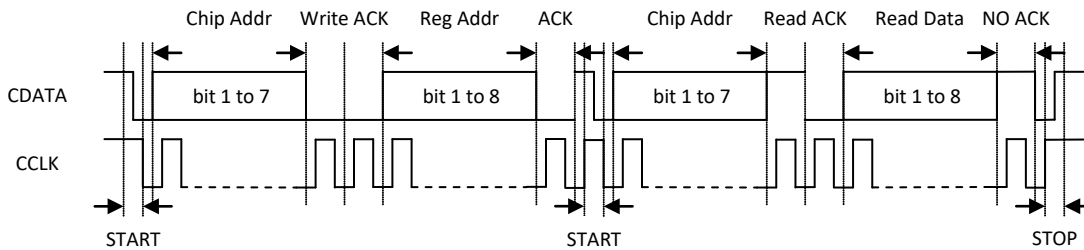


Figure 1b I²C Read Timing

4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	GND-0.3V	VDD+0.3V
Digital Input Voltage Range	GND-0.3V	VDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDD	1.7	1.8/3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDD=3.3V, GND=0V, ambient temperature=25°C, CLOCK=6.144 MHz.

PARAMETER	MIN	TYP	MAX	UNIT	
ADC Performance					
Dynamic Range (A-weight)	0 dB PGA	92	95	98	dB
	23 dB PGA	88	91	94	
	26 dB PGA	87	90	93	
	29 dB PGA	85	88	91	
	32 dB PGA	83	86	89	
THD+N (0 dB PGA)	-85	-88	-91	dB	
Channel Separation (1KHz)	102	105	108	dB	
Interchannel Gain Mismatch		0.1		dB	
Gain Error			±5	%	
Analog Input					
Full Scale Input Level		±1.0*VDD/3.3		±Vrms	
ES7202 Input Impedance		19.2 (0 dB PGA)		KΩ	

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDD=3.3V (16 kHz)		22		mW
VDD=1.8V (16 kHz)		4.6		
Power Down Mode		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*VDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		VDD		V
Output Low-level Voltage		0		V

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F _{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T _{TWID}	4.7/1.3		us
Start Condition Hold Time	T _{TWSTH}	4.0/0.6		us
Clock Low time	T _{TWCL}	4.7/1.3		us
Clock High Time	T _{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T _{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T _{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T _{TWDS}	0.25/0.1		us
Rise Time of CCLK	T _{TWR}		1.0/0.3	us
Fall Time CCLK	T _{TWF}		1.0/0.3	us

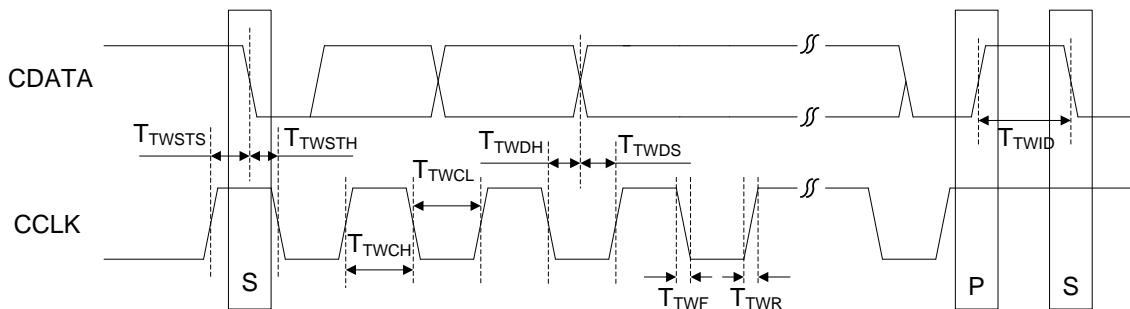


Figure 2 I²C Timing

PDM DATA SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT	
CLOCK frequency		0.512	6.144	MHz	
CLOCK duty cycle	≤ 3.072 MHz	40 45	60 55	%	
DATA valid	V _{DDD} =3.3V V _{DDD} =1.8V	T _{VALID}	11 19	27 61	ns
DATA hold	V _{DDD} =3.3V V _{DDD} =1.8V	T _{HOLD}	10 18	26 56	ns

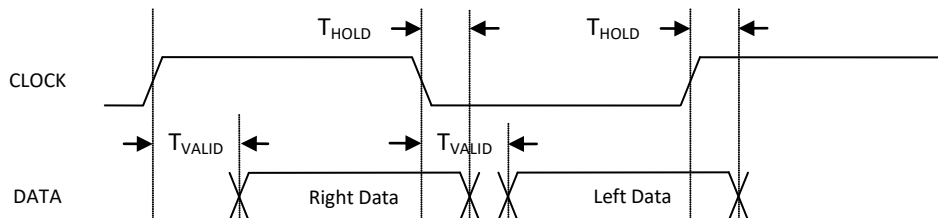
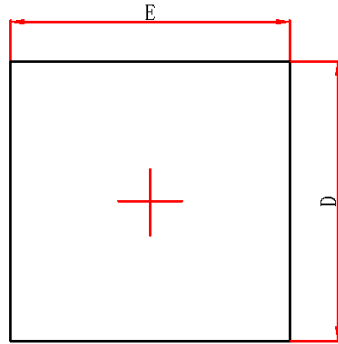


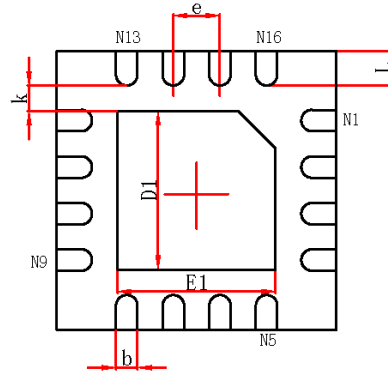
Figure 3 PDM Data Timing

5. PACKAGE

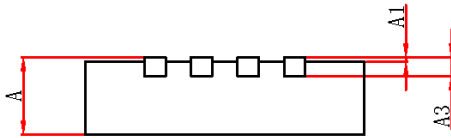
QFNWB3×3-16L (P0.50T0.75) PACKAGE OUTLINE DIMENSIONS



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.500TYP.	
L	0.300	0.500	0.012	0.020

6. CORPORATE INFORMATION

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