ES8374

Low Power Mono Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I^2S/PCM master or slave serial data port
- Two pairs of analog input with differential input option
- Mono analog output
- 256/384Fs, USB 12/24 MHz, fractional PLL for wide range of system clocks
- Standard audio clock output
- Sophisticated analog input and output routing, mixing and gain
- GPIO
- I^2C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 95 dB signal to noise ratio, -85 dB THD+N
- Low noise pre-amplifier
- Noise reduction filters
- Auto level control (ALC) and noise gate
- Support analog and digital microphone
- Microphone bias

DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 95 dB signal to noise ratio, -85 dB THD+N
- 1.25W@8Ω/5V or 1.8W@4Ω/4.2V mono class D speaker driver
- Dynamic range compression
- Headphone and external mic detection
- Pop and click noise suppression

Low Power

- 3.3V to 5V operation
- 32 mW playback; 42 mW playback and record
- Low standby current

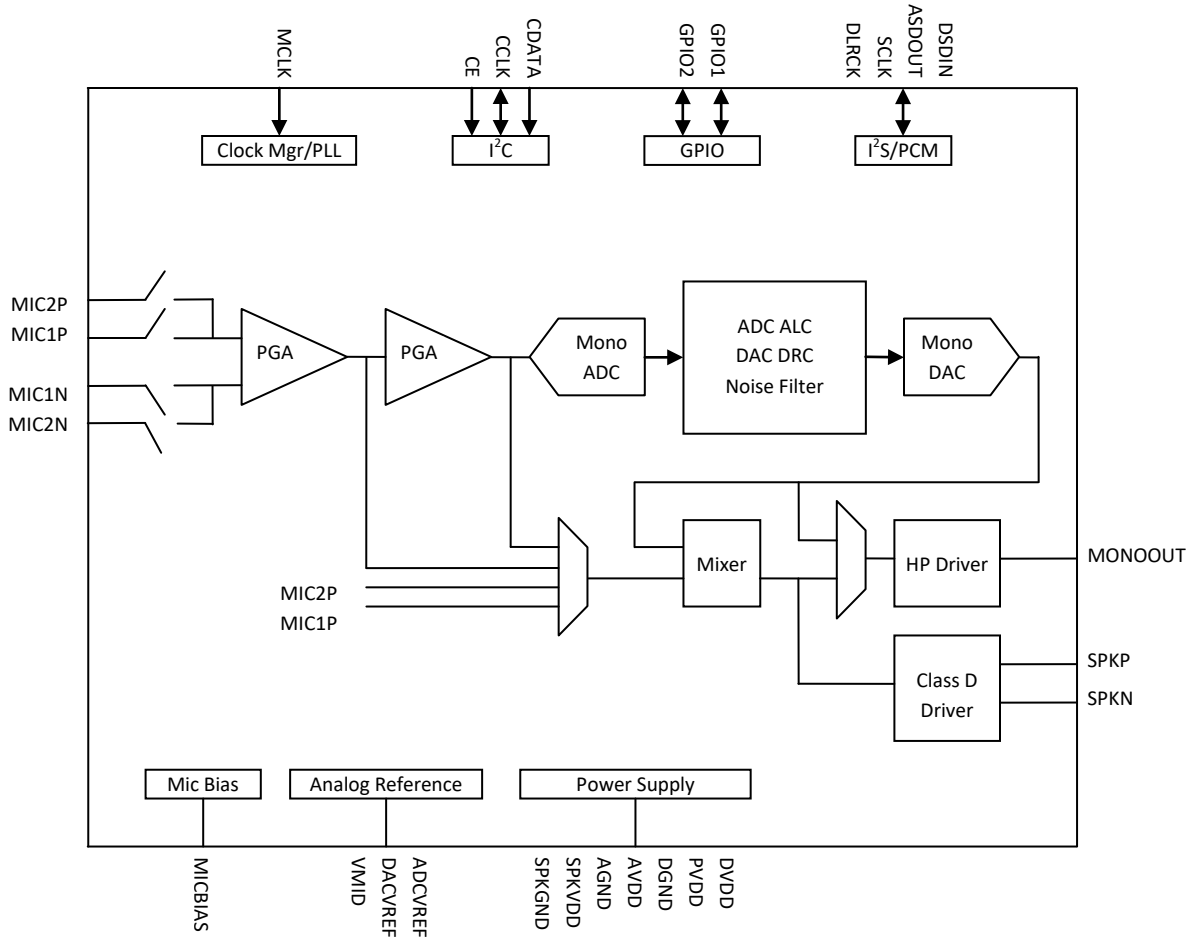
APPLICATIONS

- Car DV
- IP Camera
- DVR, NVR
- Surveillance

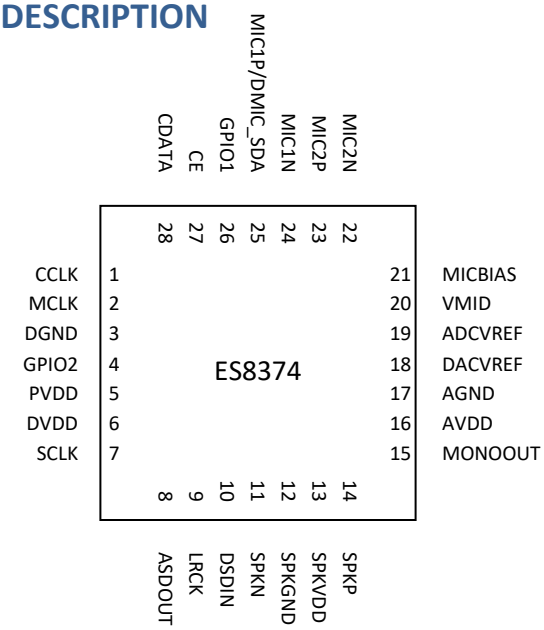
ORDERING INFORMATION

ES8374 -40°C ~ +85°C
QFN-28

1. BLOCK DIAGRAM

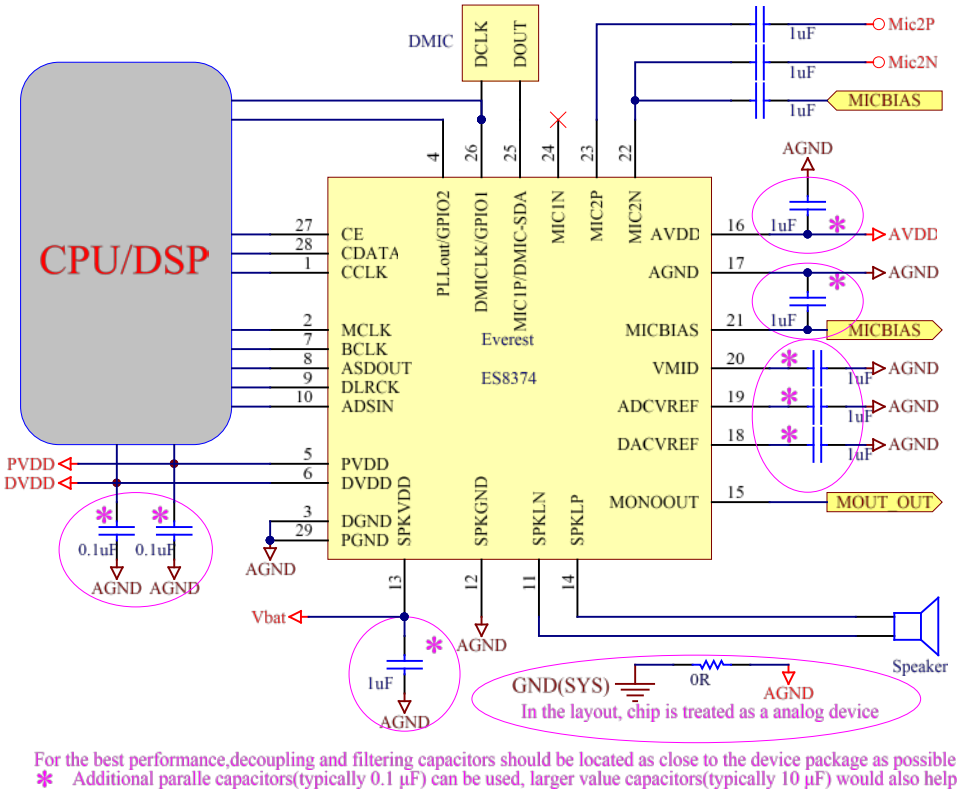


2. PIN OUT AND DESCRIPTION



NAME	I/O	DESCRIPTION
MCLK	DI	Master clock
CDATA	DIO	I^2C data
CCLK	DI	I^2C clock
CE	DI	I^2C address
GPIO1	DIO	GPIO (digital mic clock, jack detect, PLL out, interrupt)
GPIO2	DIO	GPIO (PLL out, interrupt)
ASDOUT	DO	I^2S/PCM serial data out
DSDIN	DI	I^2S/PCM serial data in
LRCK	DIO	I^2S/PCM left and right clock
SCLK	DIO	I^2S/PCM bit clock
MIC1P/DMIC_SDA	AI	P analog input or digital mic data
MIC1N	AI	N analog input
MIC2P	AI	P analog input
MIC2N	AI	N analog input
MONOOUT	AO	Mono output
SPKP	AO	Positive speaker out
SPKN	AO	Negative speaker out
MICBIAS		Mic bias
ADCVRP		ADC reference filtering
DACVRP		DAC reference filtering
VMID		Common mode filtering
DVDD		Digital core power supply
PVDD		Digital IO power supply
DGND		Digital ground
AVDD		Analog power supply
AGND		Analog ground
SPKVDD		Speaker driver power supply
SPKGND		Speaker driver ground

3. TYPICAL APPLICATION CIRCUIT



4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports three types of clocking: standard audio clocks (256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and an on-chip 22-bit fractional PLL clock.

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I²C interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 400 kbps.

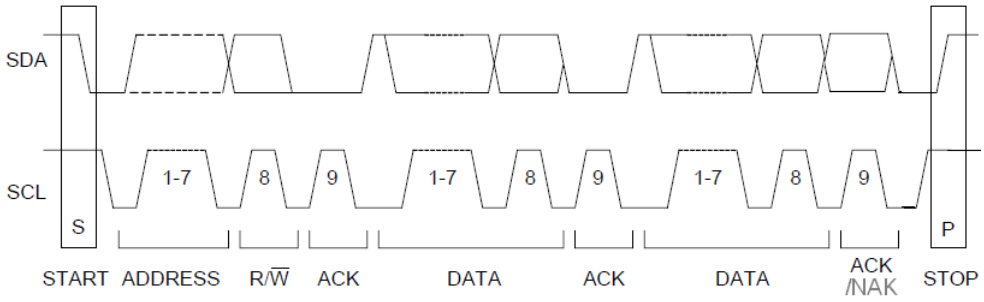


Figure 1 Data Transfer for I²C Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In I²C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I²C Interface Mode

Chip Address		R/W		Register Address		Data to be written
001000	AD0	0	ACK	RAM	ACK	DATA

Table 2 Read Data from Register in I²C Interface Mode

Chip Address		R/W		Register Address
001000	AD0	0	ACK	RAM
Chip Address		R/W		Data to be read
001000	AD0	1	ACK	Data

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, BCLK (SCLK) and DACDAT/ADCDAT pins. These formats are I^2S, left justified, right justified, DSP/PCM and TDM mode. DAC input DACDAT is sampled by the device on the rising edge of SCLK. ADC data is out at ADCDAT on the falling edge of SCLK. The relationship of SDATA (DACDAT/ADCDAT), SCLK and LRCK with these formats are shown through Figure 2 to Figure 6.

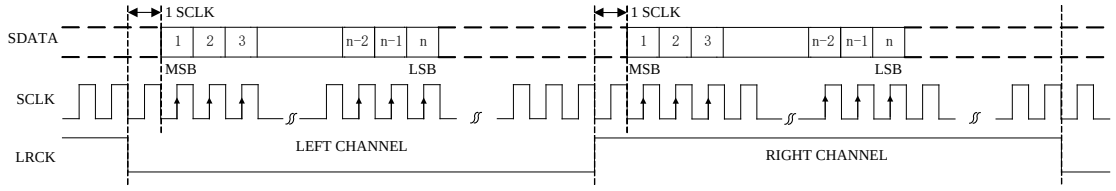


Figure 2 I^2S Serial Audio Data Format Up To 24-bit

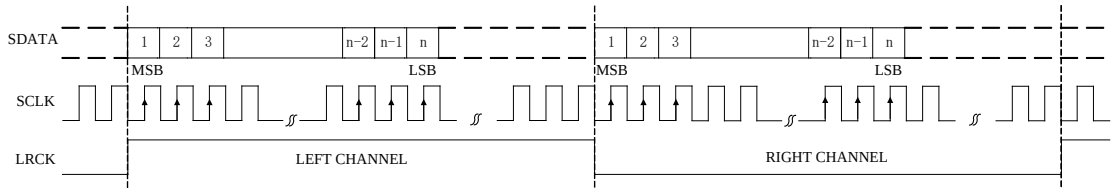


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

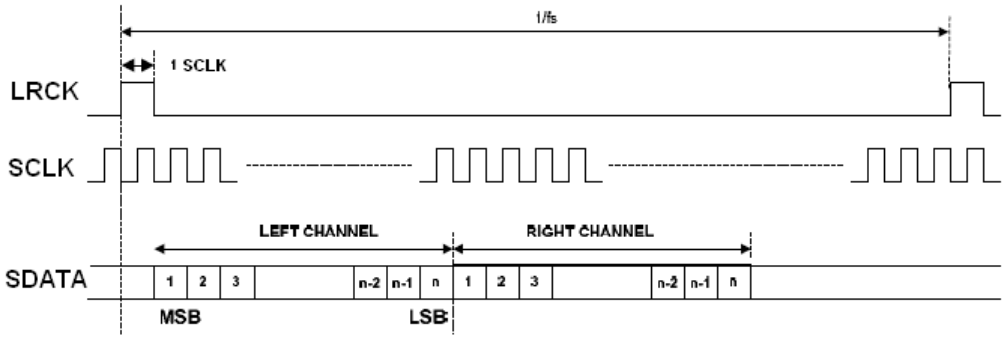


Figure 4 DSP/PCM Mode A

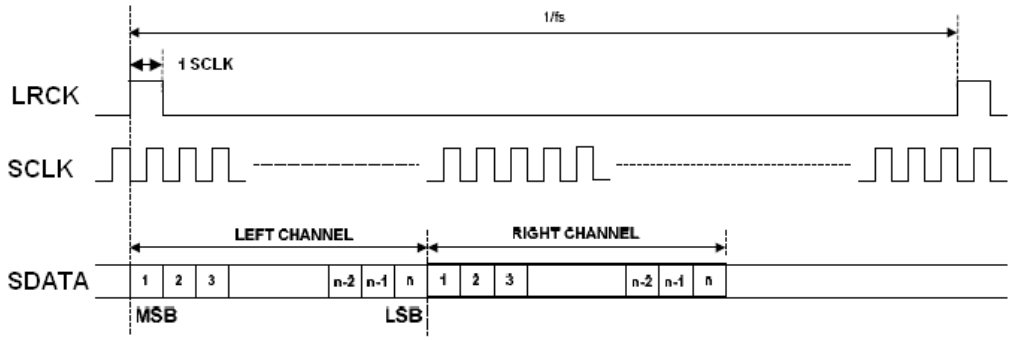


Figure 5 DSP/PCM Mode B

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+5.5V
Digital Supply Voltage Level	-0.3V	+5.5V
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
AVDD	3	3.3/5	5.5	V
SPKVDD (Note 1, 2) 4Ω Speaker 8Ω Speaker	 3 3	 3.3/4.2 3.3/5	 5 5.5	V
DVDD	3	3.3/5	5.5	V
PVDD (DVDD - input high level < 2V)	1.6	1.8/3.3/5	5.5	V

Note 1: package thermal pad must be connected to ground as much as possible to provide class D speaker driver heat dissipation.

Note 2: when standby class D speaker driver, with all power supply on, entering low power through control register setting, then stopping MCLK.

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz or 96 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	85	95	98	dB
THD+N	-88	-85	-75	dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	50			dB
Filter Frequency Response – Double Speed				
Passband	0		0.2268	Fs
Stopband	0.4535			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	50			dB
Analog Input				
Full Scale Input Level		±AVDD/3.3		±Vrms
Input Impedance		10		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz or 96 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	83	95	98	dB
THD+N	-88	-85	-75	dB
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	56			dB
Analog Output				
Full Scale Output Level		AVDD/3.3		Vrms

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=3.3V, PVDD=3.3V, AVDD=3.3V: Play back Play back and record		 32 42		mW
Power Down Mode				
DVDD=3.3V, PVDD=3.3V, AVDD=3.3V		50		uA
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	TSCLKL	15		ns
SCLK Pulse width high	TSCLKH	15		ns
SCLK falling to LRCK edge	TSLR	–10	10	ns
SCLK falling to SDOUT valid	TSDO	0		ns
SDIN valid to SCLK rising setup time	TSDIS	10		ns
SCLK rising to SDIN hold time	TSDIH	10		ns

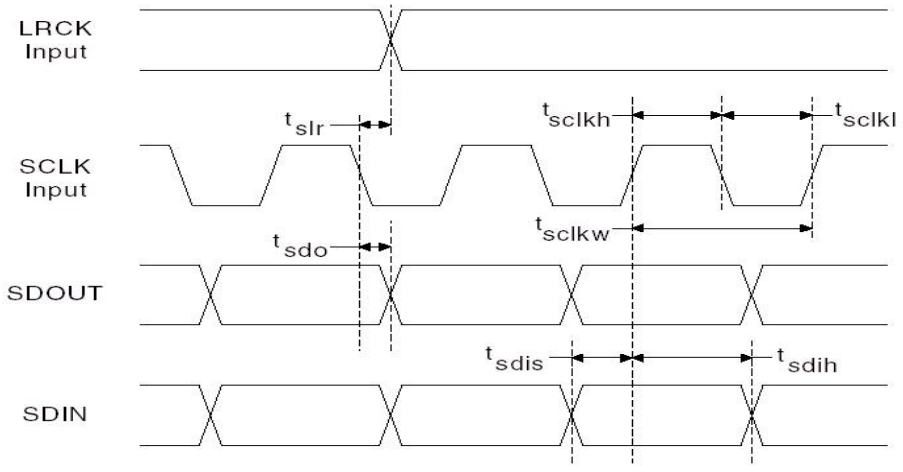


Figure 6 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

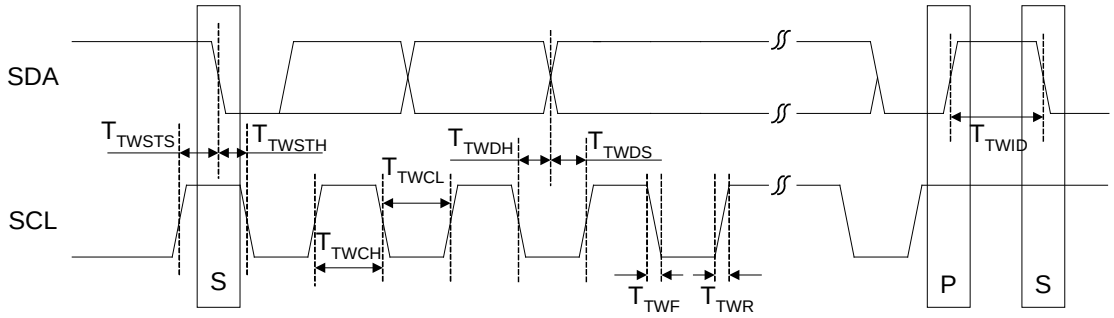
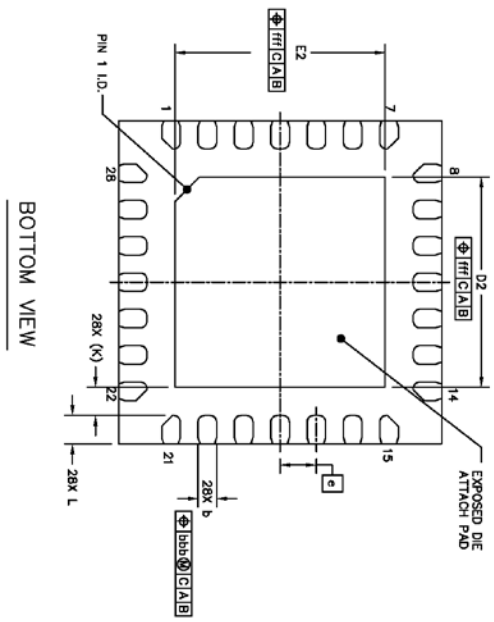
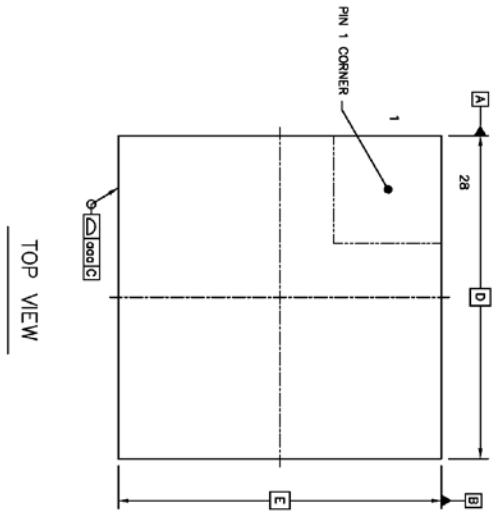
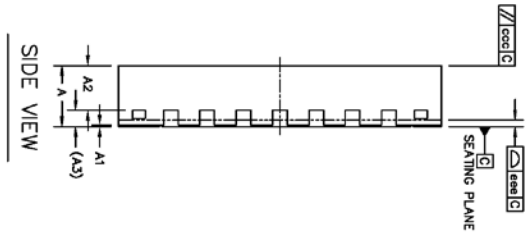


Figure 7 I²C Timing

8. PACKAGE (UNIT: MM)







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.18	0.23	0.28
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.45 BSC	
EP SIZE	X	D2	2.5	2.6	2.7
	Y	E2	2.5	2.6	2.7
LEAD LENGTH		L	0.25	0.35	0.45
LEAD TIP TO EXPOSED PAD EDGE		K		0.35 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

9. CORPORATE INFORMATION

Everest Semiconductor Co., Ltd.

苏州工业园区金鸡湖大道 1355 号国际科技园, 邮编 215021

Email: info@everest-semi.com

10.IMPORTANT NOTICE AND DISCLAIMER

Everest Semiconductor publishes reliable technical information about its products. Information contained herein is subject to change without notice. It may be used by a party at their own discretion and risk. Everest Semiconductor disclaims responsibility for any claims, damages, costs, losses, and liabilities arising out of your use of the information. This publication is not to be taken as a license to operate under any existing patents and intellectual properties.